MOSFETs mit high-k Gate-Dielektrika

Bernhard Fabel
Lehrstuhl für Technische Elektronik, TU München

1. Bayerischer FORNEL-Workshop, 12. April 2005

Outline

- ❒ Motivation
- ❒ high-*k* dielectrics
- ❒ MOS–Technology
- ❒ Al_2O_3
- ❒ Pr_2O_3
- ❒ Evaluation
- ❒ Summary

Motivation – Introduction

CMOS shrink

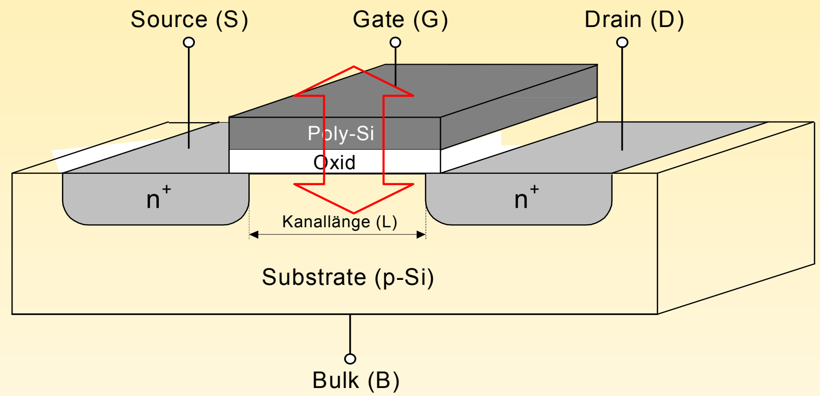
⇒ Thinner gate oxides

⇒ Tunneling current

i) increasing power consumption

ii) reduced device life time

Leakage current through gate stack

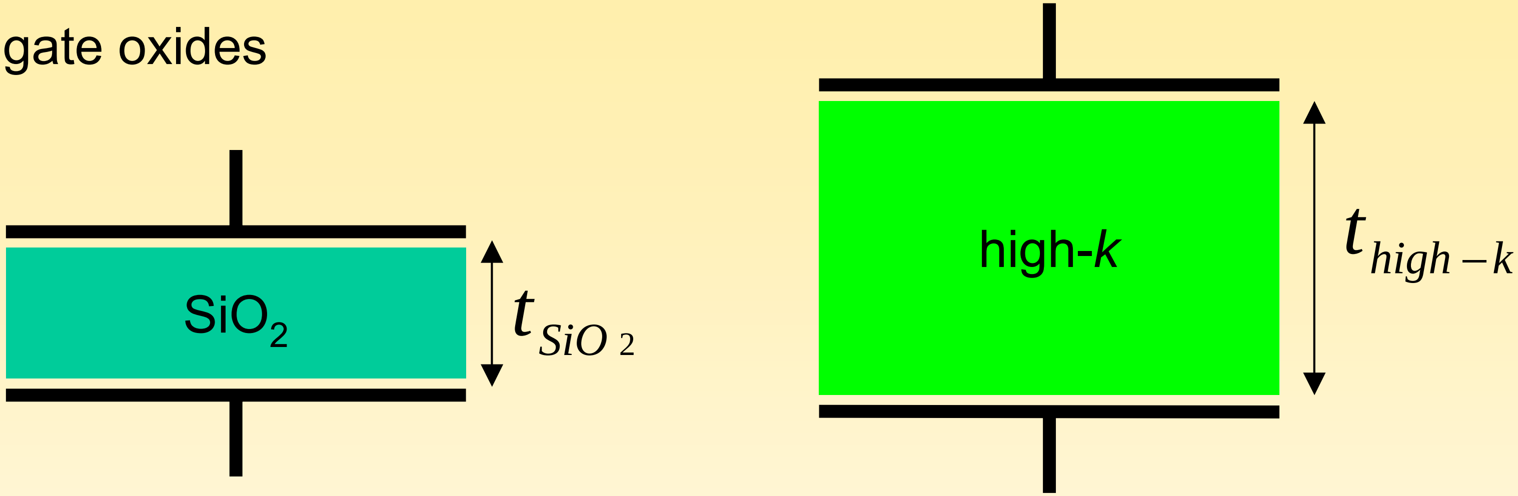


tunneling oxide < 4nm phy. thickness

ITRS 2003

Year		2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
T. Node (nm)		130	115	100	90	80	70	65	45	32	22
EOT (nm)	MPU/ASIC	1.3–16	1.2–1.5	1.1–1.6	0.9–1.4	0.8–1.3	0.7–1.2	0.6–1.1	0.5–0.8	0.4–0.6	0.4–0.5
	LOP	2.0-24	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4	0.8-1.2	0.7-1.1	0.6-1.0
	LSTP	2.4-2.8	2.2-2.6	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	0.9-1.3	0.8-1.2	07-1.1
	DRAM	5	4,5	4,1	3,6	3,3	3	2,7	1,55	1,05	0,55

Solution: thicker gate oxides



$$\frac{\varepsilon_o \cdot \varepsilon_{SiO_2} \cdot A}{t_{SiO_2}} = C_{Ox} = \frac{\varepsilon_o \cdot \varepsilon_{high-k} \cdot A}{t_{high-k}}$$

$$\varepsilon \uparrow \Rightarrow t_{Insulator} \uparrow \Rightarrow C = konst.$$

→ Reduction of tunneling current

high-*k* - Requirements

Relative permittivity: $\varepsilon_{r,high\text{-}k} = 12 – 20$ **3.9**

=> Equivalent oxide thickness $$EOT = t_{eq} = t_{high-k} \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}}$$

	high-*k* requirements	SiO_2
❒ Break through voltage	E_{BD} > 5 MV/cm	10 MV/cm
❒ Interface state density	$D_{it} < 10^{11}$ /eVcm²	$5*10^{11}$ /eVcm²
❒ Band gap energy	E_G > 5 eV	9 eV
❒ *n*-Channel mobility	μ ~ 600 cm²/Vs	670 cm²/Vs
❒ CMOS compatibility	yes	yes
❒ … and many more	…	…

high-*k* → **Nearly as good as Silicon oxide SiO_2 in all features**

High-*k* – Materials studied

Al_2O_3

- Low rel. permittivity ε_r = 7.2...11

+ good properties:
    1. E_{BD} > 6.2...7.2 MV/cm
    2. $D_{it} < 10^{11}$ /eVcm^2
    3. E_G > 8.3...8.8 eV

+ ALD System available

+ mobility μ unknown!

Pr_2O_3

+ good values Monocrystalline:
    1. rel. permittivity ε_r
    2. Leakage current

+ no data for amorphous films

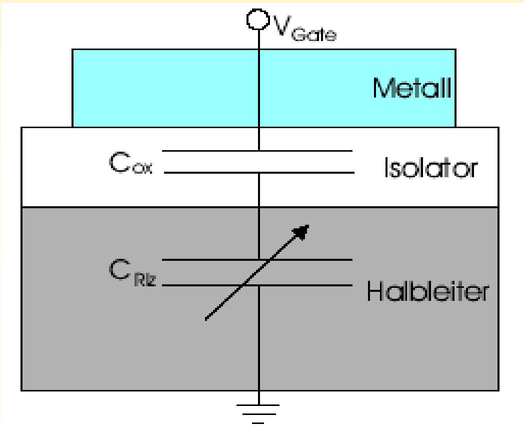
+ mobility μ unknown!

MOS-Technology

On silicon oxid SiO_2

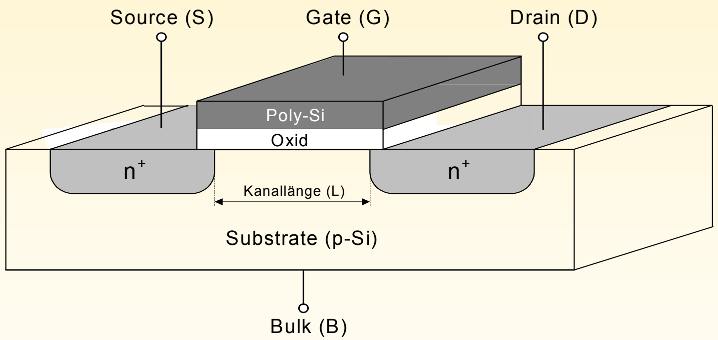
MOS – Diodes

- 1 Chromium-Mask process
- 7344 structures per wafer



n-MOSFETs

- 5 Chromium-Mask process
- 501 MOSFET per wafer
- 5 aspect ratios W/L

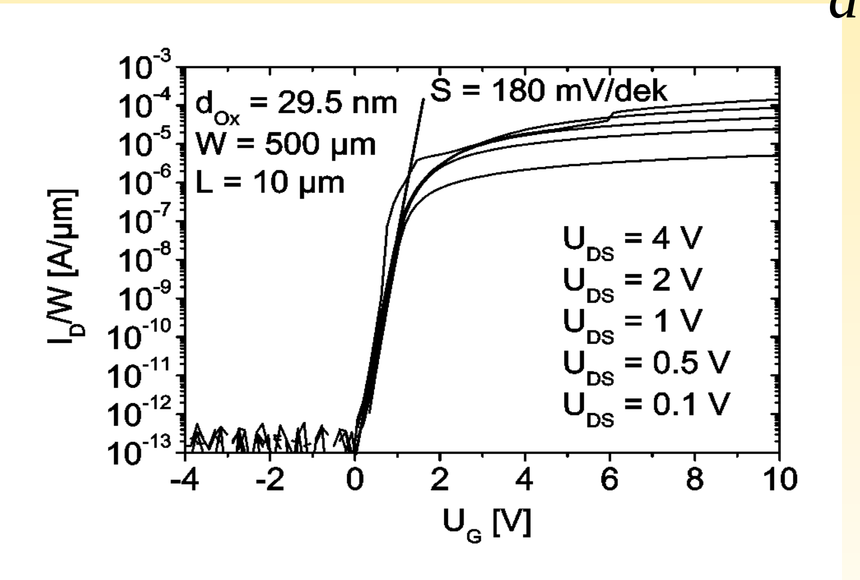


MOS-Diodes and MOSFETs with aluminium gate metal

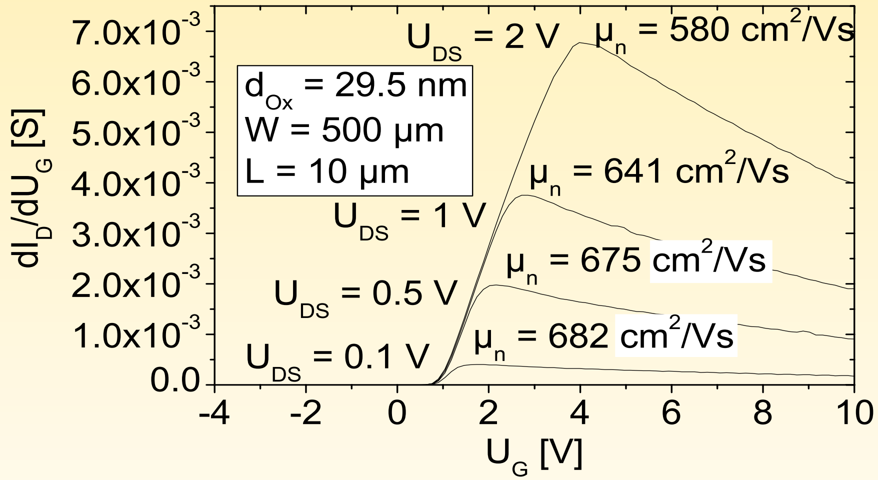
n-MOSFET Parameters (SiO_2)

$$\frac{dI_D}{dU_D}$$

Transfer-Characteristics



Mobility



- Subthreshold swing: S = 180 mV/dek
- Off Current per Micron W: $I_{off} = 10^{-13}$ A/µm

- *n*-Channel Mobility:

  $\mu = 682\ cm^2/Vs$ @ $V_{DS} = 0.1V$

!Industry values!

Al_2O_3 - Deposition

Friedrich-Alexander-Universität Erlangen-Nürnberg
Institut für Technische Physik
Lehrstuhl für Experimentalphysik

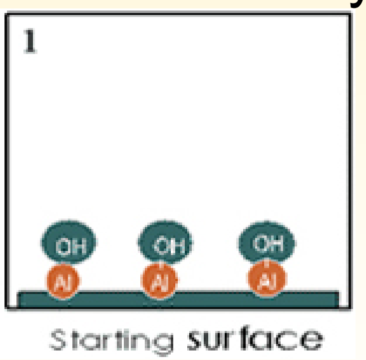
ALD with

1. Water vapor H_2O
2. Tetramethylaluminium (TMA) $Al(CH_3)_3$

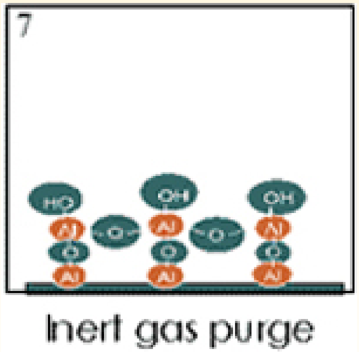
@ p = 1mbar and 300°C

$$2Al(CH_3)_3 + 3H_2O \xrightarrow{300^\circ C} Al_2O_3 + 6CH_4$$

monolayer by monolayer



1x gas purge



ASM Microchemistry Ltd.

F120 SAT

Al_2O_3 – MIS Parameters

Data extracted from C(V)- and J(V)-Plots

•rel. Permittivity:

$\varepsilon_r = 9.12$

• EOT ~ 8.3 nm

• Interface state density:

$D_{it} = 5*10^{11}$ /eVcm²

• Flatband voltage shift:

$\Delta V_{FB1} = -0.41V$

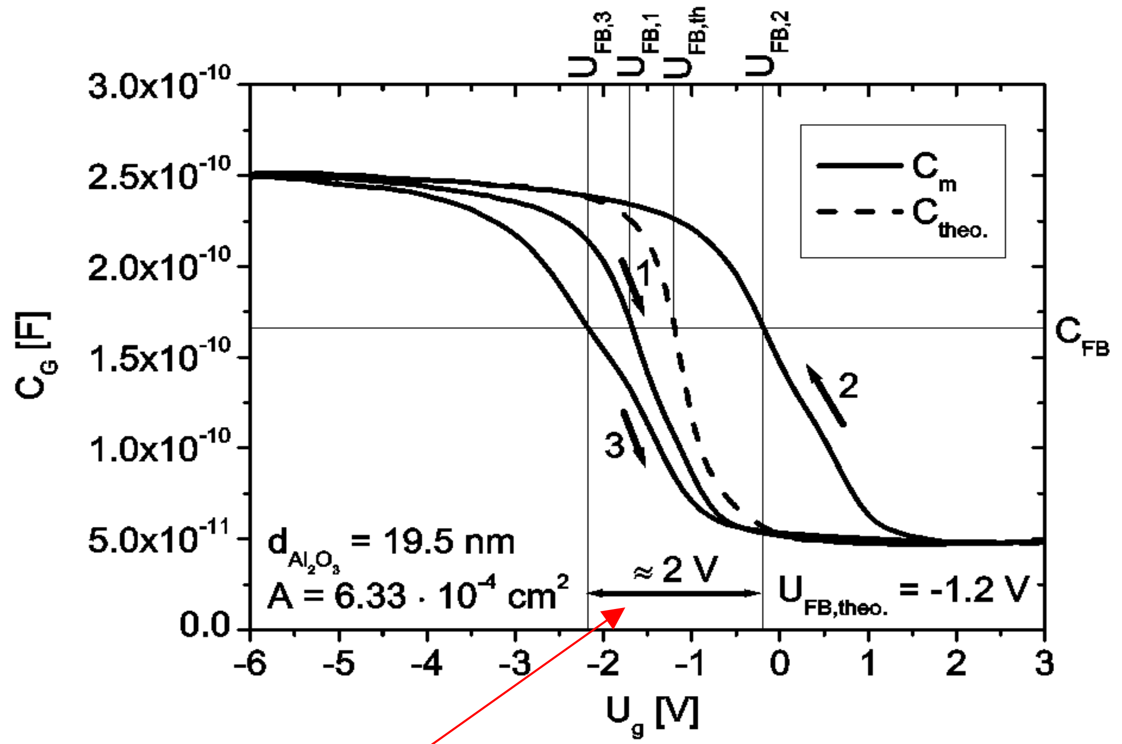
$\Delta V_{FB2} = +0.98V$

$\Delta V_{FB3} = -0.81V$

•Break through voltage:

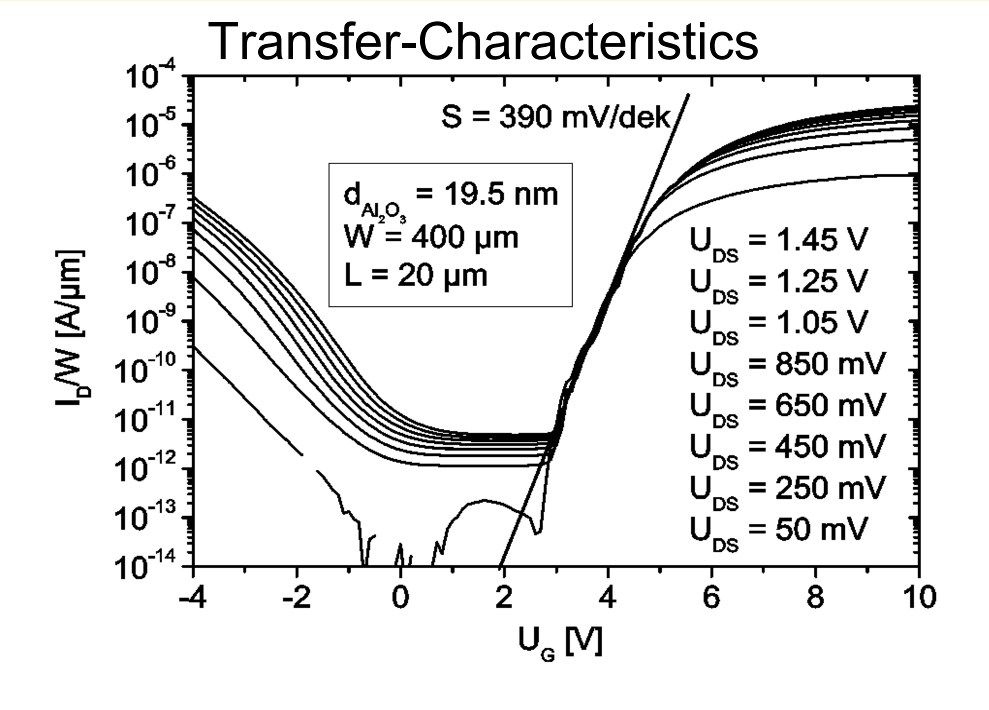
$E_{BD} = 5.8$ MV/cm

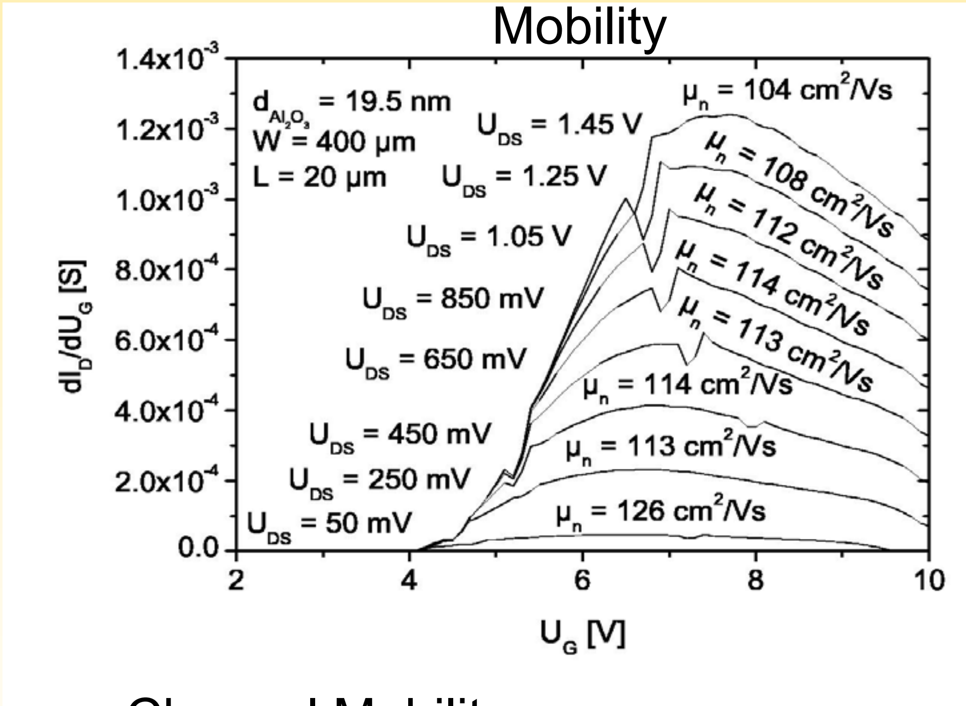
Capacitance-Voltage Plot



strong hysteresis

n-MISFET Parameters (Al_2O_3)





- Subthreshold swing: S = 390 mV/dek
- Off Current per Micron W: $I_{off} = 10^{-12}$ A/µm
- *n*-Channel Mobility:

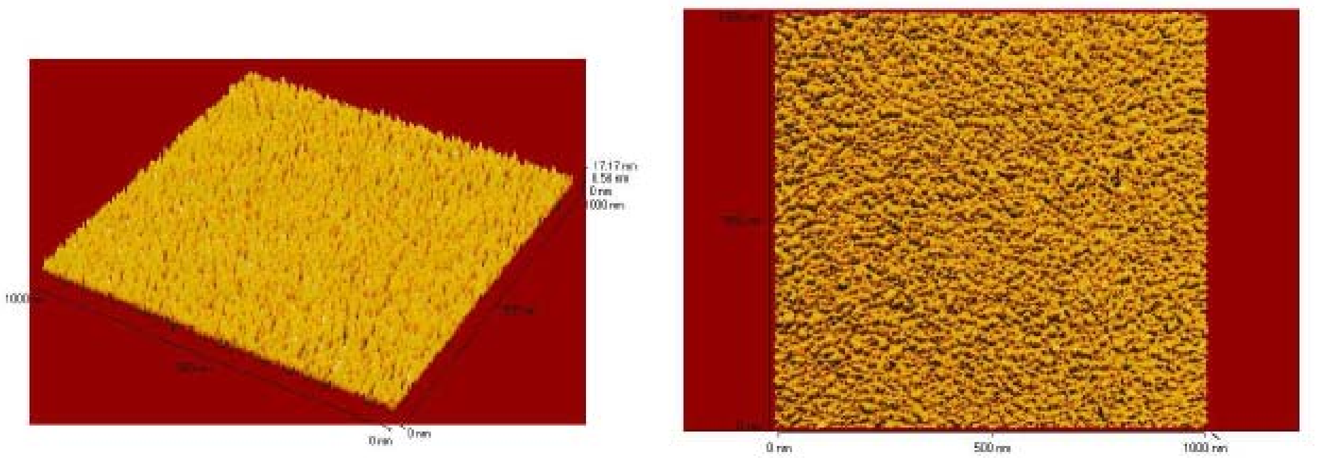
  $\mu = 126\ cm^2/Vs$ @ $V_{DS} = 0.05V$

Pr_2O_3 - Deposition

Molecular Beam Evaporation

- in ultra high vacuum
- @ RT and 10^{-7} mbar
- Precursor: Pr_2O_3

amorphous films —700°C→ poly crystalline



(a) Seitenansicht (b) Draufsicht

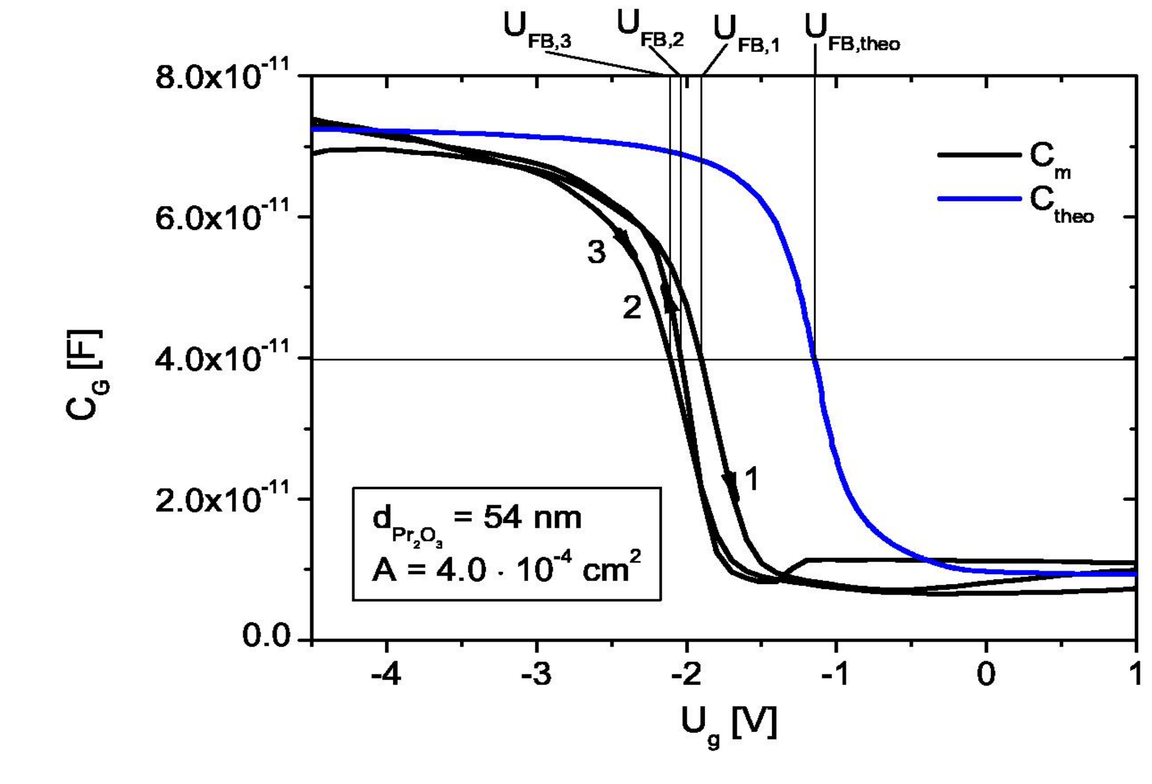
AFM pictures showing a amorphous Pr_2O_3 film (1x1 µm²)

Pr_2O_3 - MIS-Structures

Data extracted from C(V)- and J(V)-Plots

- rel. Permittivity:
  $\varepsilon_r = 11.0$
- EOT ~ 19.1 nm
- Interface state density:
  $D_{it} = 1.4 \cdot 10^{12}$ /eVcm²
- Flatband voltage shift:
  $\Delta V_{FB1} = -0.47V$
  $\Delta V_{FB2} = -0.63V$
  $\Delta V_{FB3} = -0.70V$
- Break through voltage:
  $E_{BD} = 3.0...6.5$ MV/cm

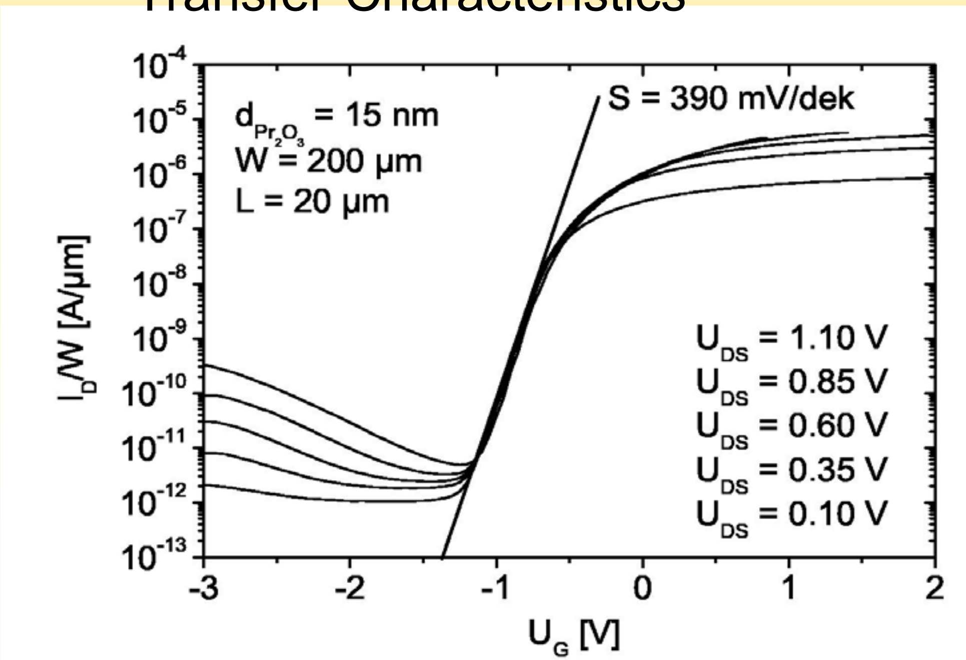
Capacitance-Voltage Plot



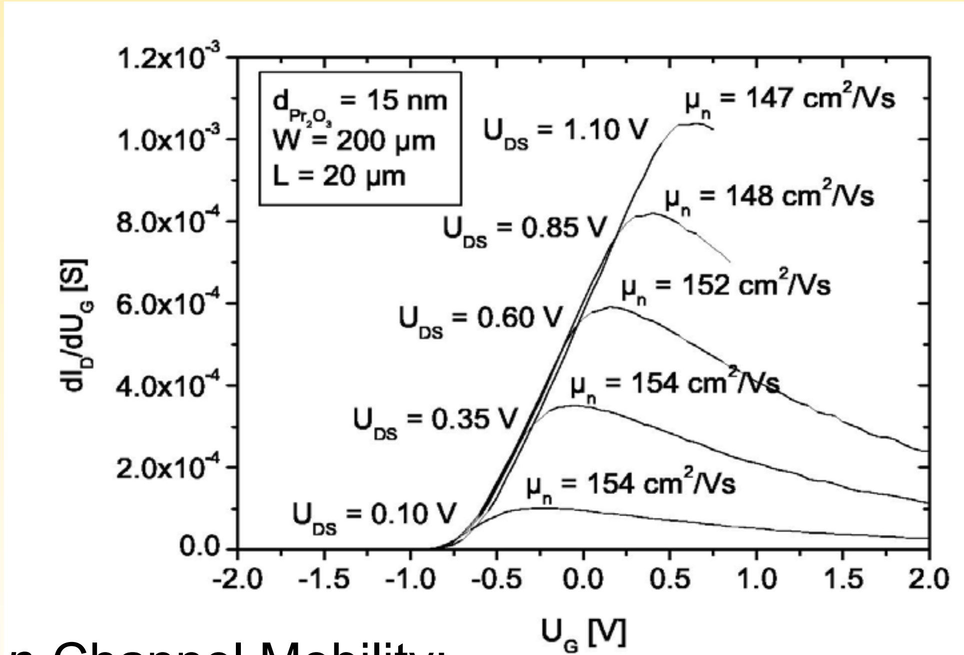
High leakage current for smaller films

n-MISFET Parameters (Pr_2O_3)

Transfer-Characteristics



Mobility



- Subthreshold swing: S = 390 mV/dek
- Off Current: $I_{off} > 2.0*10^{-12}$ A/µm

- *n*-Channel Mobility:

  $\mu = 154\ cm^2/Vs$ @ $V_{DS} = 0.1V$

Evaluation

	Subthreshold swing [mV/dek]	Off Current [A/µm]	*n*-Channel Mobility [cm^2/Vs]
Reference SiO_2 MOSFETs	180	10^{-13}	682
Al_2O_3 MOSFETs	390	10^{-12}	~126
Pr_2O_3 MOSFETs	390	$2.0*10^{-12}$	~154

- Unsatisfying results concerning
  - Subthreshold swing
  - *n*-Channel Mobility
- Could be optimized
- Big gap to SiO_2 values!

Summary

- A reference SiO_2 MOSFETs Prozess developed with
  - Industry values
  - Aluminium metal gate

- Investigation of high-k MIS-Diodes and MISFETs with
  - Al_2O_3 ALD => hysteresis Problems
  - Pr_2O_3 amorphous MBE UHV => High leakage current, nonstable +700°C

- Very low values for
  - *n*-Channel Mobility
  - Subthreshold swing

} Al_2O_3 and Pr_2O_3