Analogschaltungen mit Tunneltransistoren

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1. Bayerischer FORNEL-Workshop, 12. April 2005

Outline

- Motivation
- TFET – device
- Basic analog circuits
  - Current mirrors
  - OTA
- Alternative circuit design: multi-V_T
- Conclusion and outlook

Motivation

The TFET is an advantageous add-on / alternative to the standard MOSFET in analog (and digital) circuit design for low-voltage, low-power applications.

Why ?

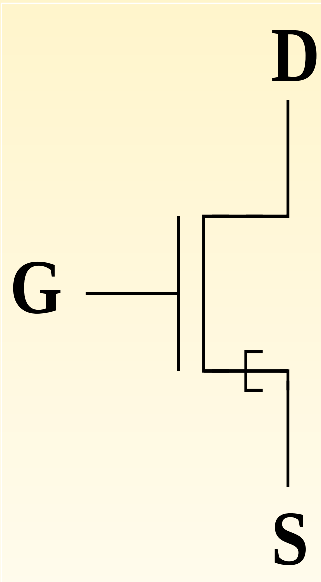
- Decreased short channel effects (e.g. DIBL) due to principle of operation

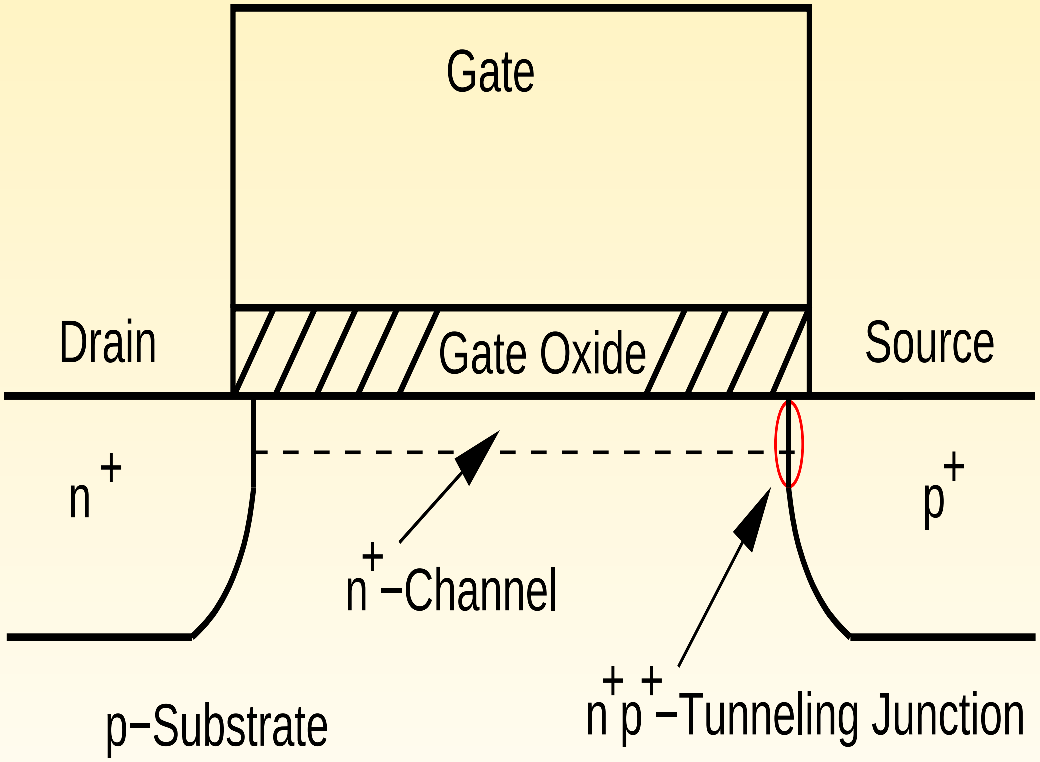
  $\Rightarrow$ **Improved analog device properties**

- Alternative circuit design: multi V_T without additional process steps
- CMOS compatible in process flow and functionality

Device

- MOS-gated pin-diode
- Off: reverse biased pin-diode
- On: tunneling junction between channel and source
- n-channel TFET:





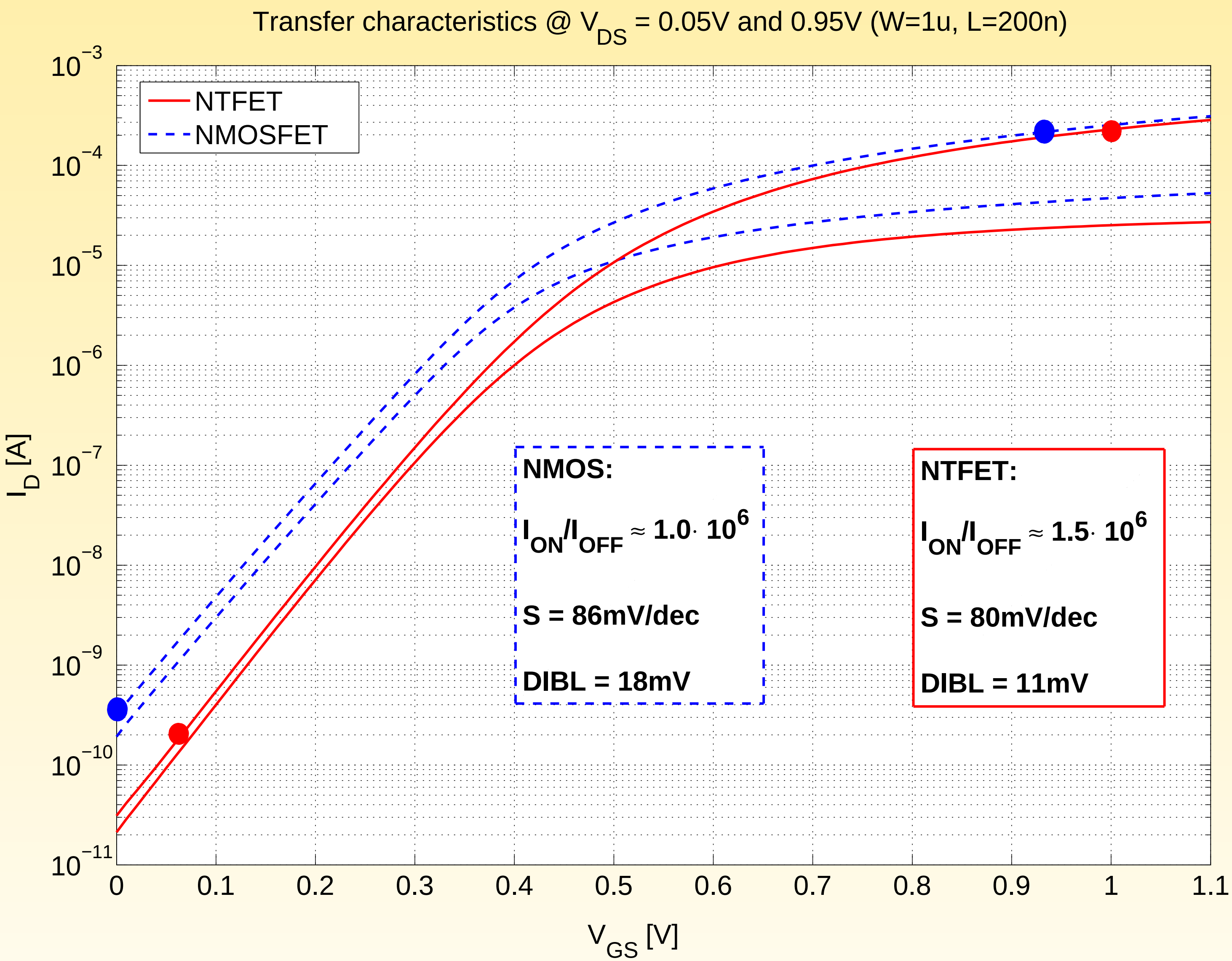
TFET Fabrication in 65nm Process

- Features of 65nm process

Technology node	65
L_{poly} (drawn)	65nm
Metal Layers	10 Cu low-k
Gate Dielectric	nitrided SiO_2
Gate Material	predoped poly Si

- Standard CMOS process flow without modifications used for fabrication of TFET
- CMOS process flow optimized for LSTP/LOP ITRS targets

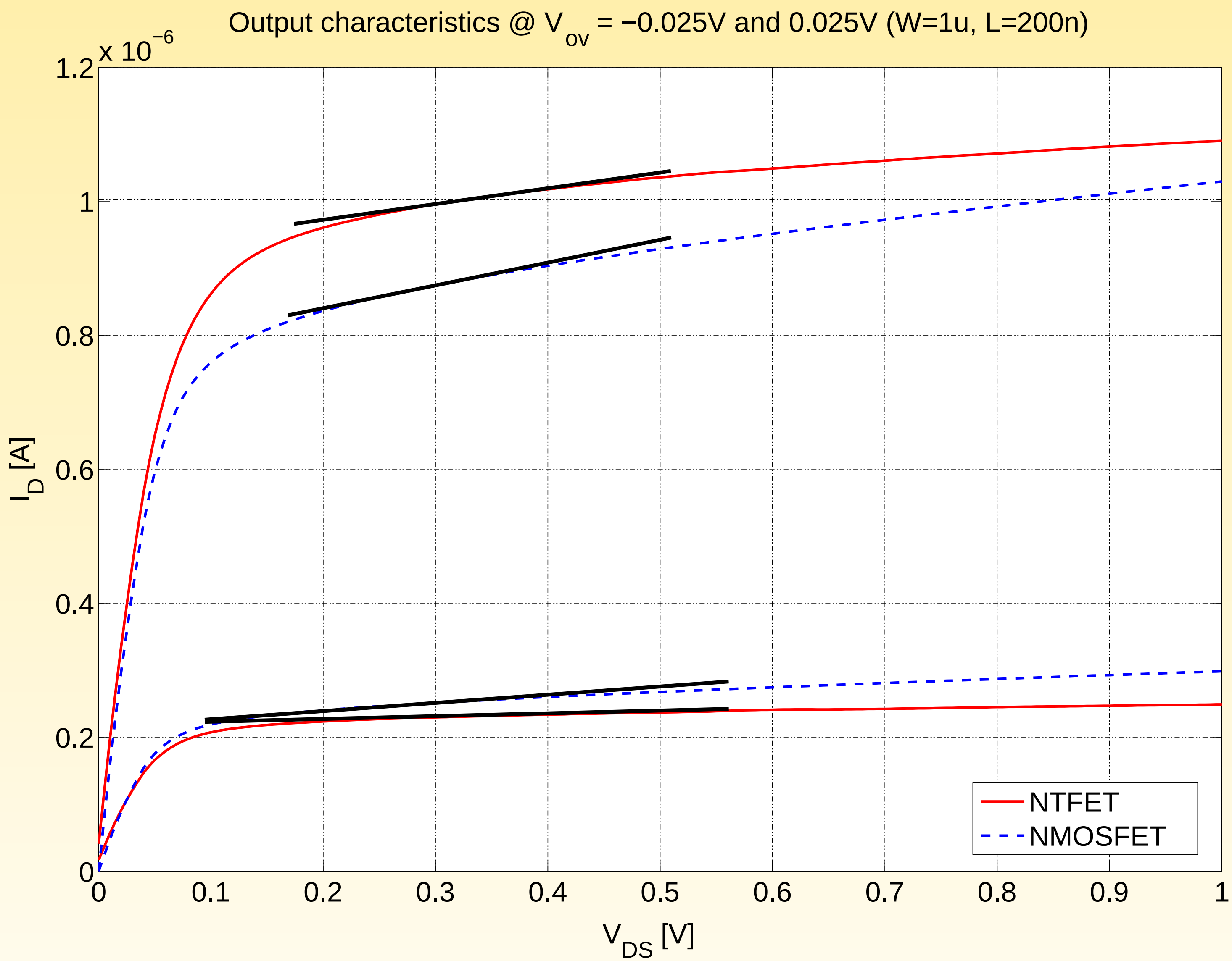
I-V Characteristics: Transfer



⇒ **Decreased short channel effects**

I-V Characteristics: Output

$V_{OV} = V_{GS} - V_T$

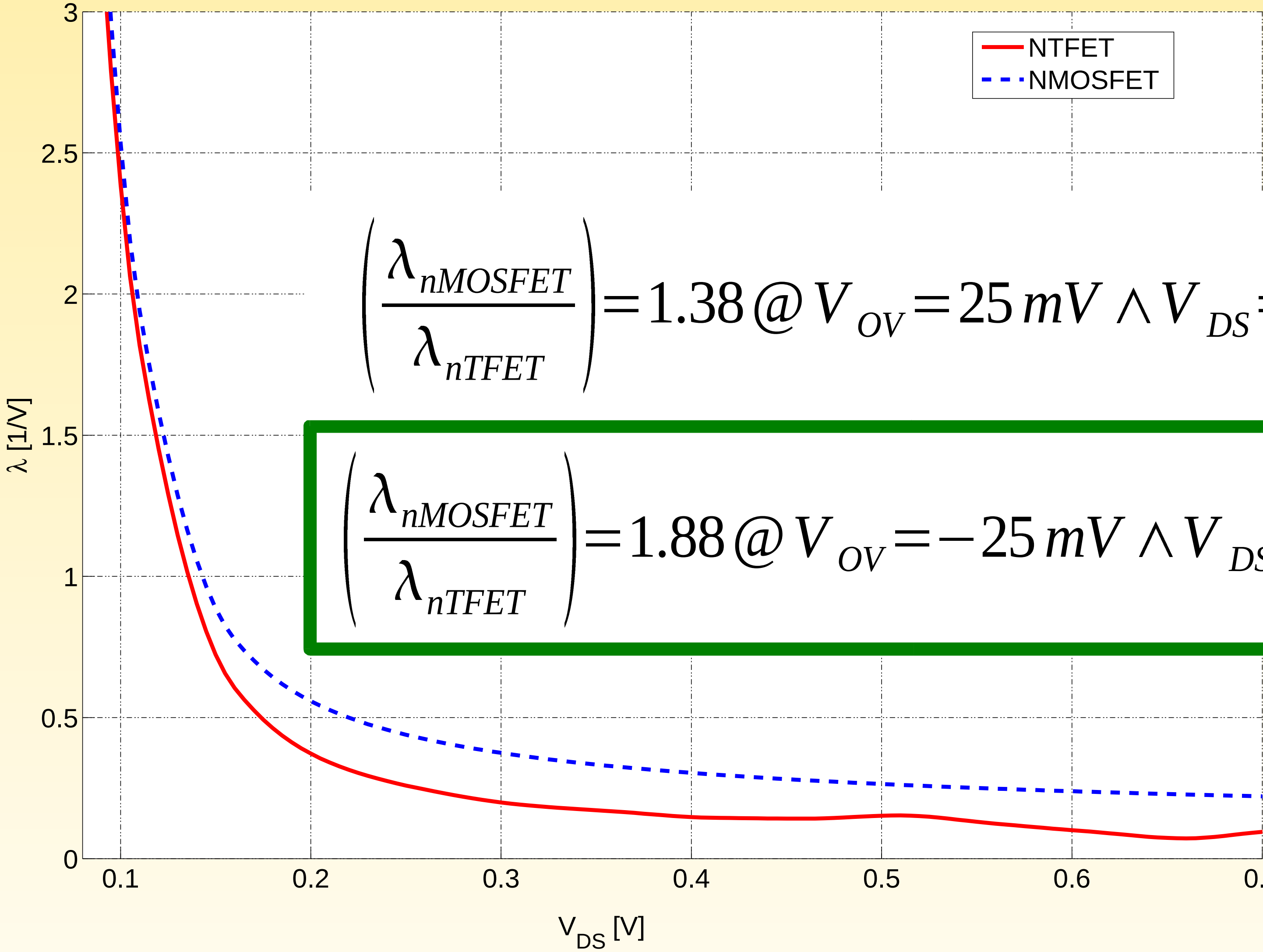


$\Rightarrow$ **Improved output resistance**

Small signal parameter: g_{DS}/I_D

$$\lambda = \frac{g_{ds}}{I_D}$$

Output conductance to current ratio @ V_{ov} = −25mV (W=1u, L=200n)



$$\left(\frac{\lambda_{nMOSFET}}{\lambda_{nTFET}}\right) = 1.38 \,@\, V_{OV} = 25\,mV \wedge V_{DS} = 0.3\,V$$

$$\left(\frac{\lambda_{nMOSFET}}{\lambda_{nTFET}}\right) = 1.88 \,@\, V_{OV} = -25\,mV \wedge V_{DS} = 0.3\,V$$

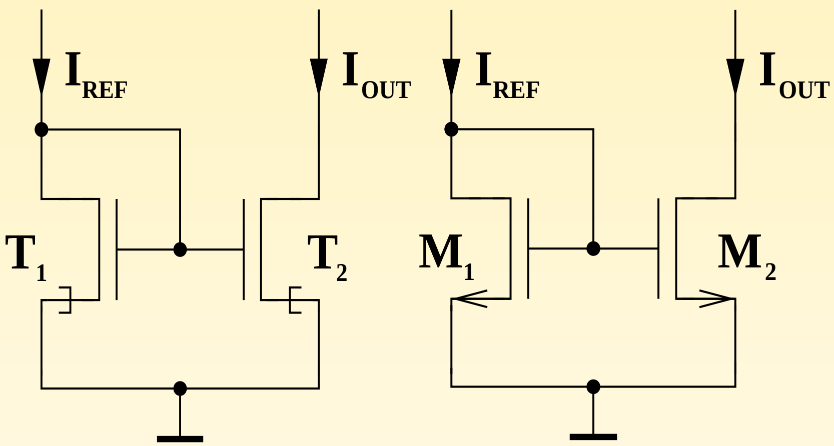
⇒ Improved output conductance to current ratio λ

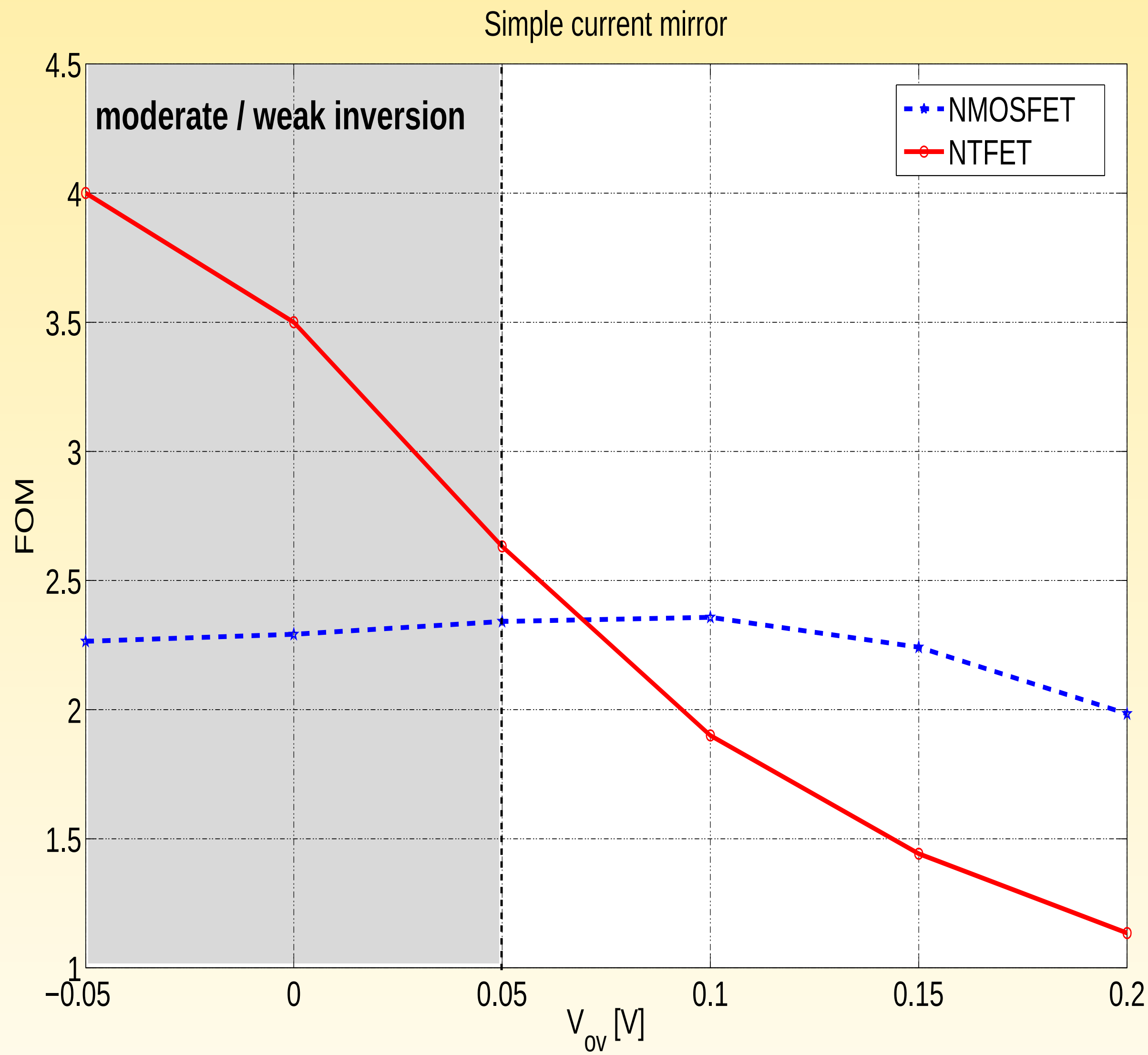
Basic Analog Circuits: Current Mirrors

Figure of merit:

$$FOM = r_{OUT} \cdot I_{OUT} \, (V^{-1})$$

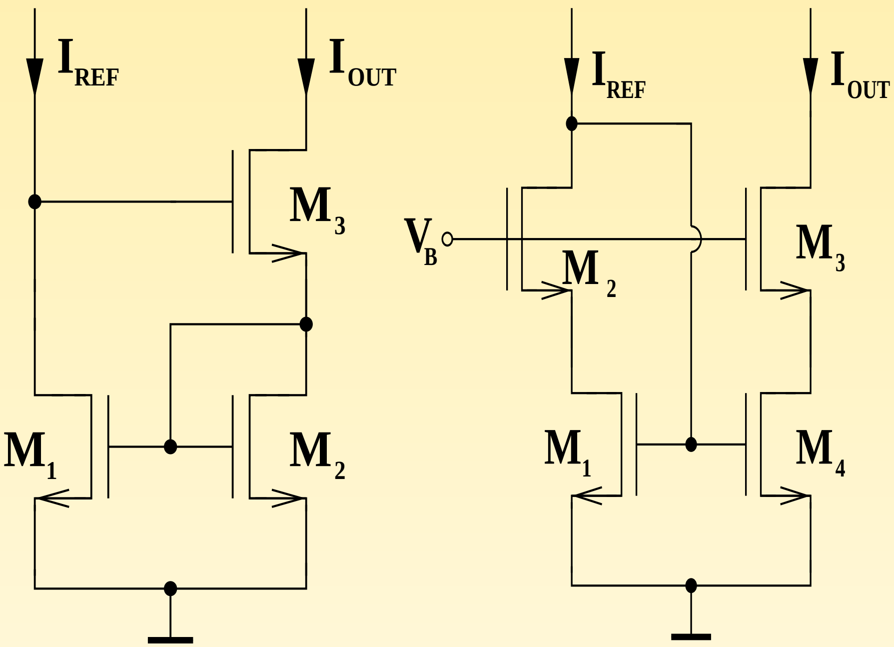
Simple current mirror

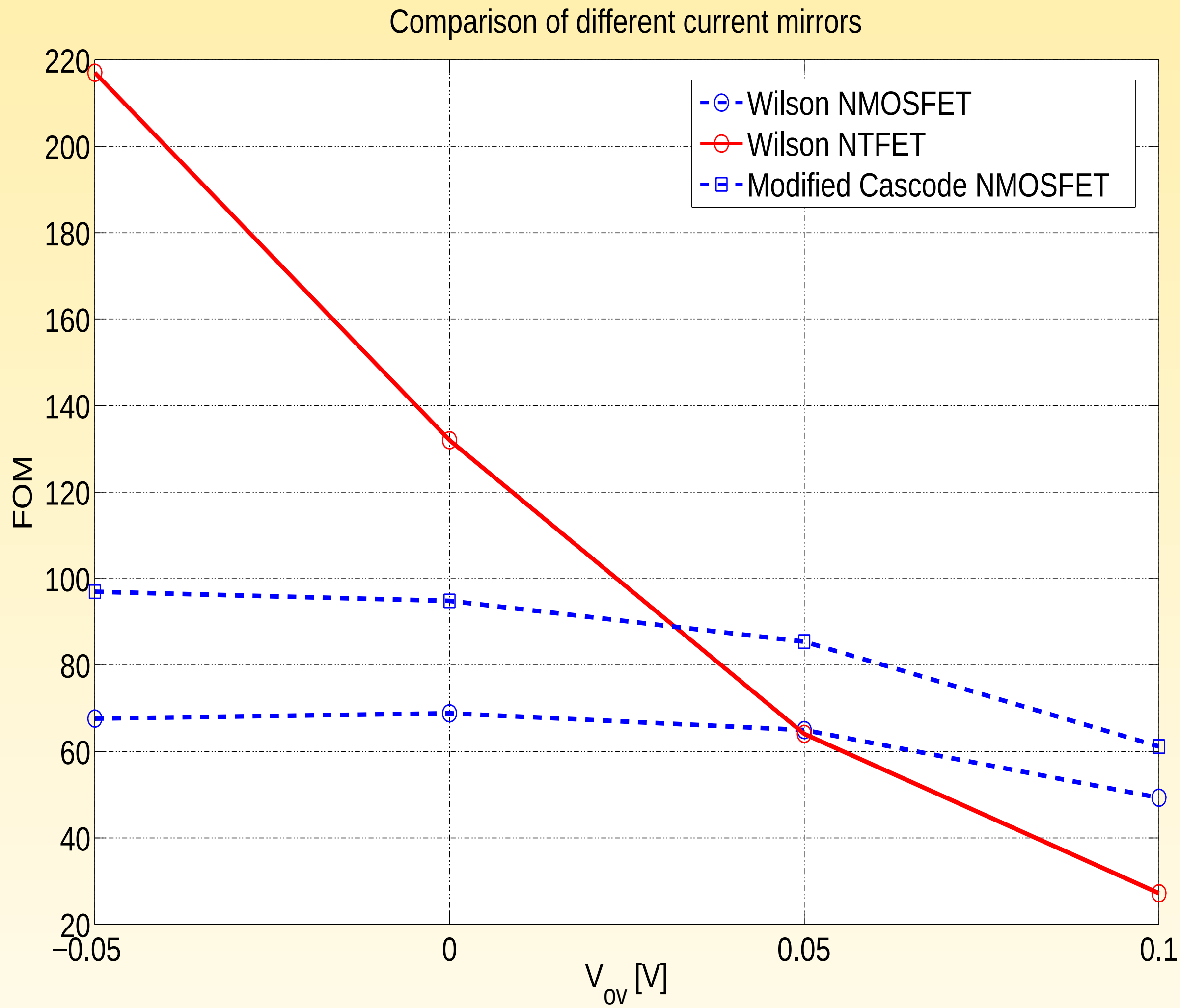




⇒ **Simple replacement of MOSFETs by TFETs improves circuit properties when transistors are biased in moderate / weak inversion**

Wilson and modified cascode current mirror

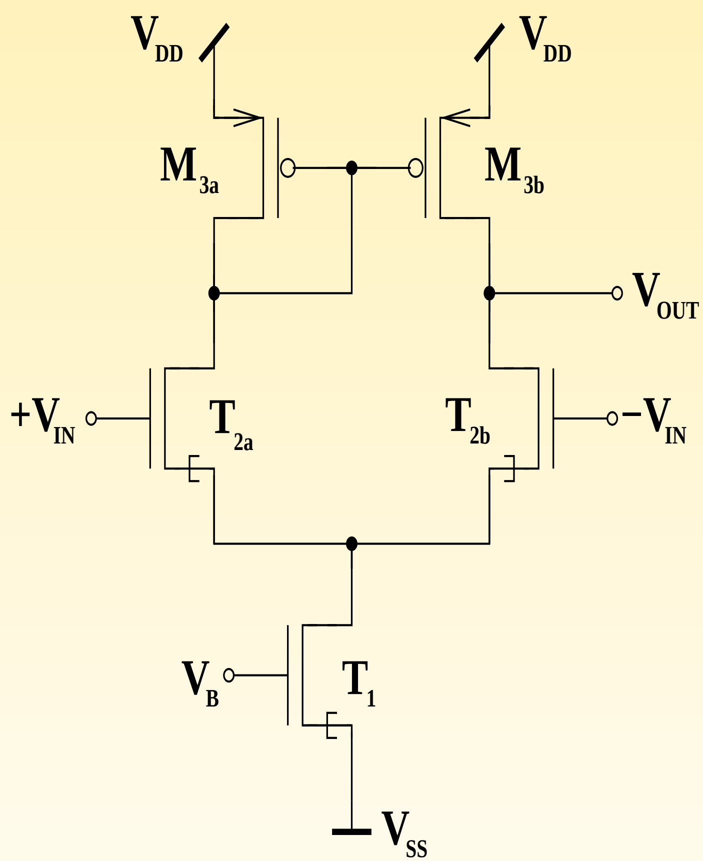




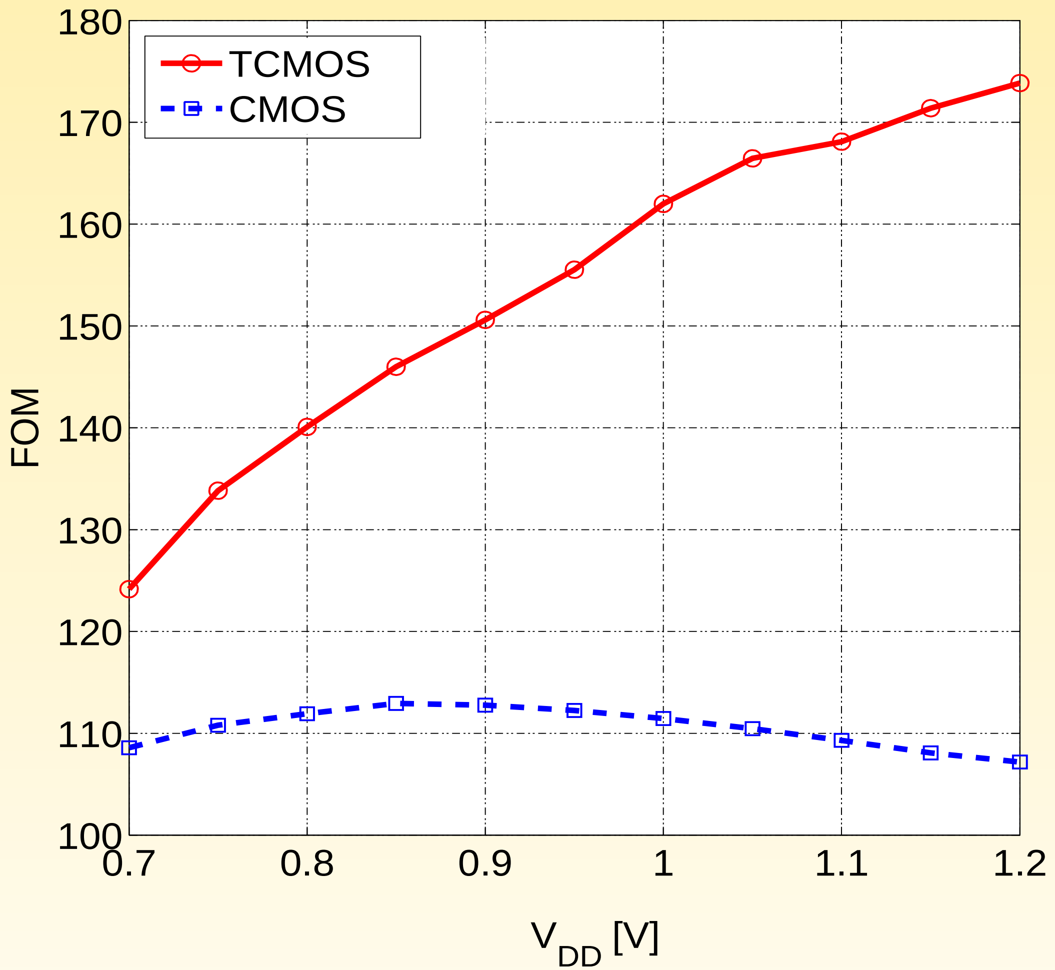
- NTFET Wilson current mirror has equal/higher FOM than NMOSFET modified cascode current mirror
- Resistance requirements can be fulfilled with less devices and without additional V_B (drawback is higher minimum V_{OUT})

$\Rightarrow$ Additional degree of freedom in circuit design

- NMOS devices replaced by NTFETs: **TCMOS**
- Transistors biased in moderate inversion (V_{OV} = 20mV)



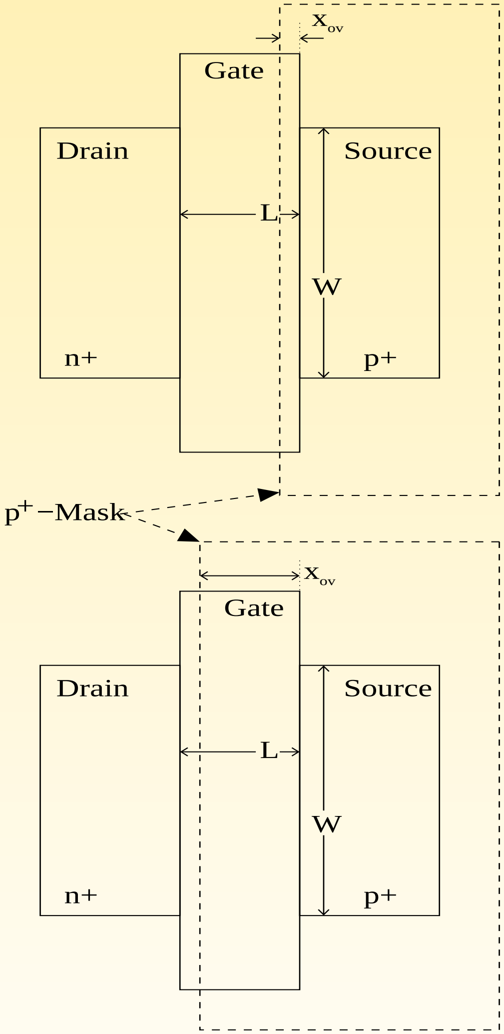
- Figure of merit: $FOM = A_{v0}\dfrac{GBW}{P}$

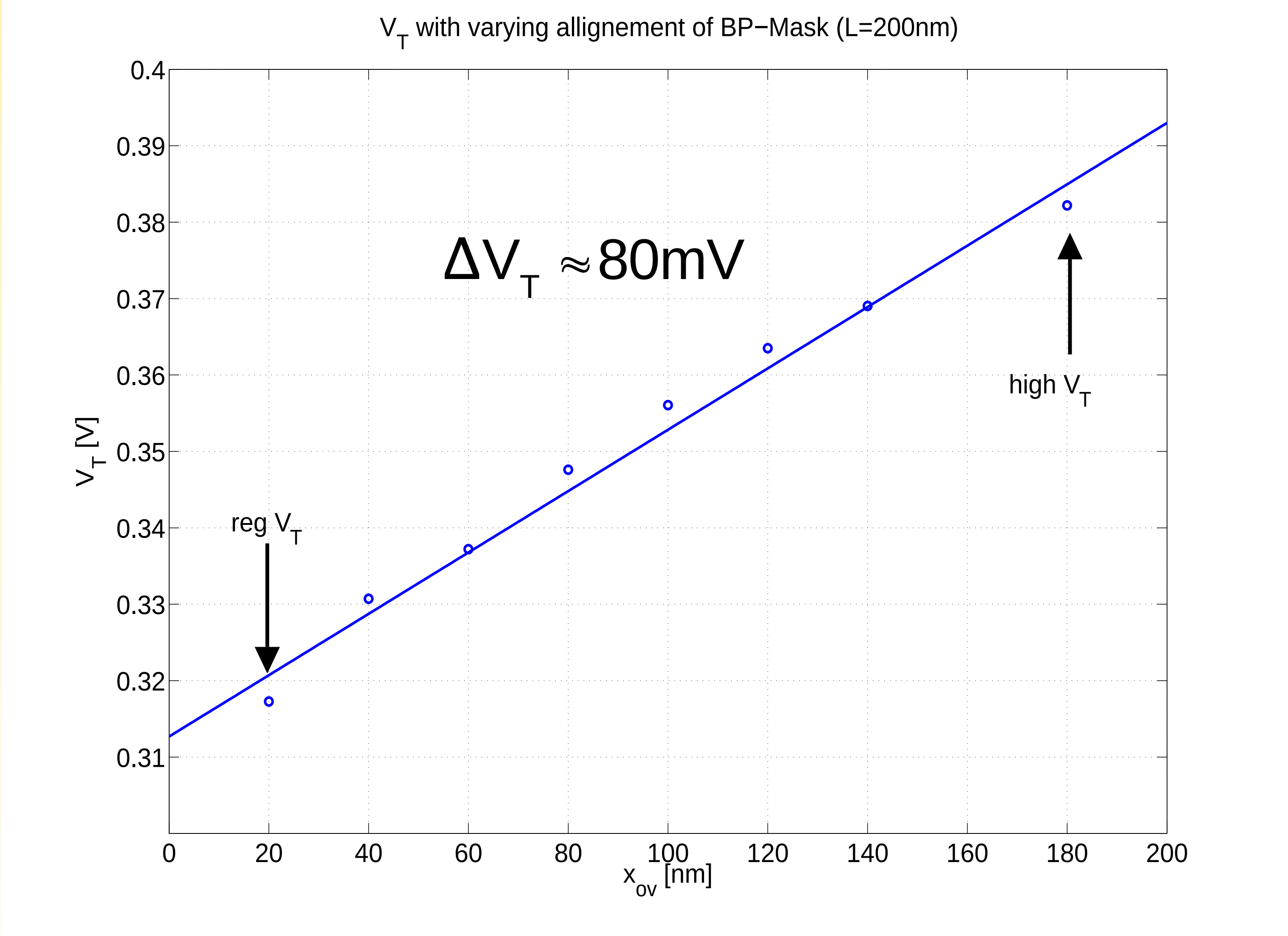


⇒ **TCMOS exhibits increased FOM (factor 1.3 @ V_{DD}= 0.8V)**

Multi-V_T Option

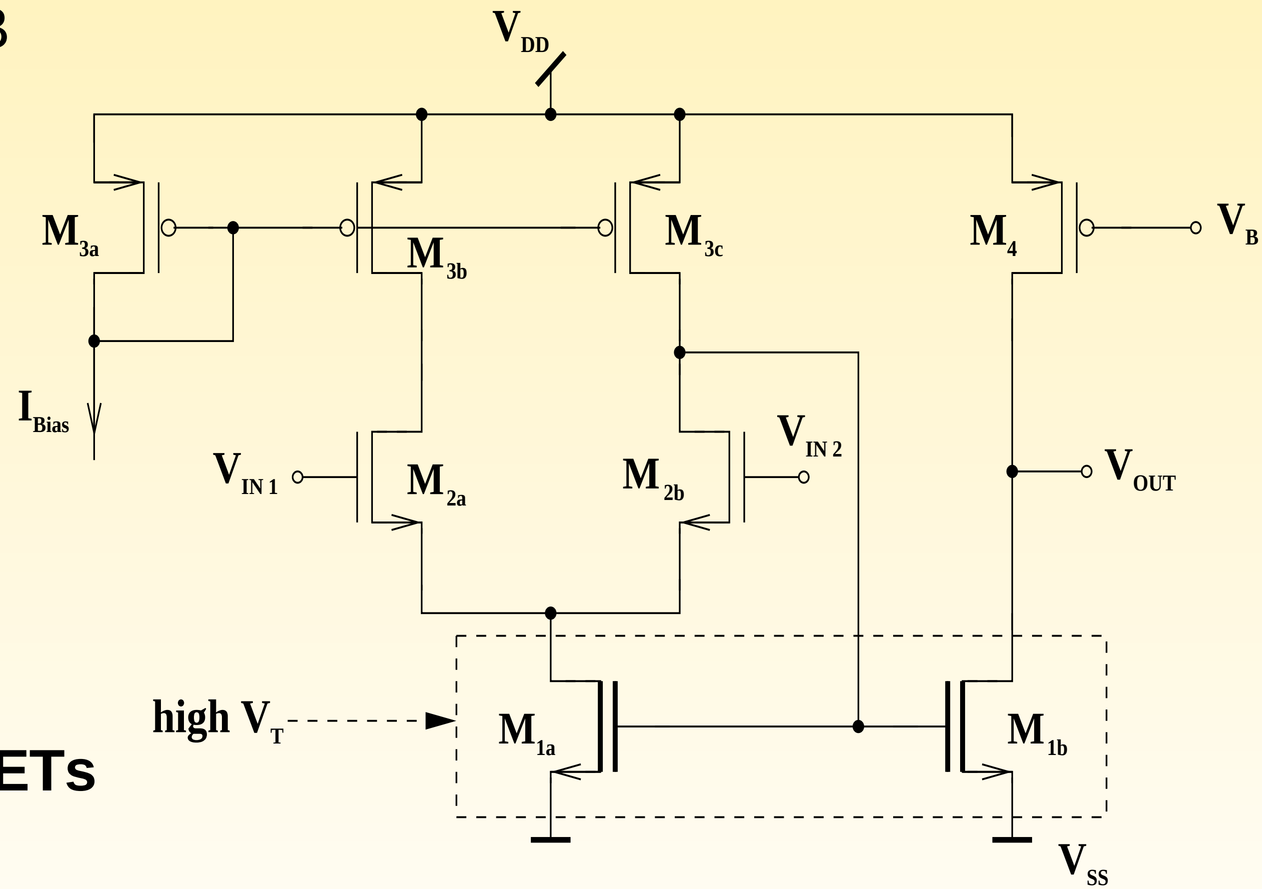
- V_T is adjustable by alignment of p+-mask, **no additonal process steps needed**
- Statistics: $\sigma_{VT\ (MOSFET)} \approx \sigma_{VT\ (MOSFET)}$





Dual-V_T Differential Input Stage

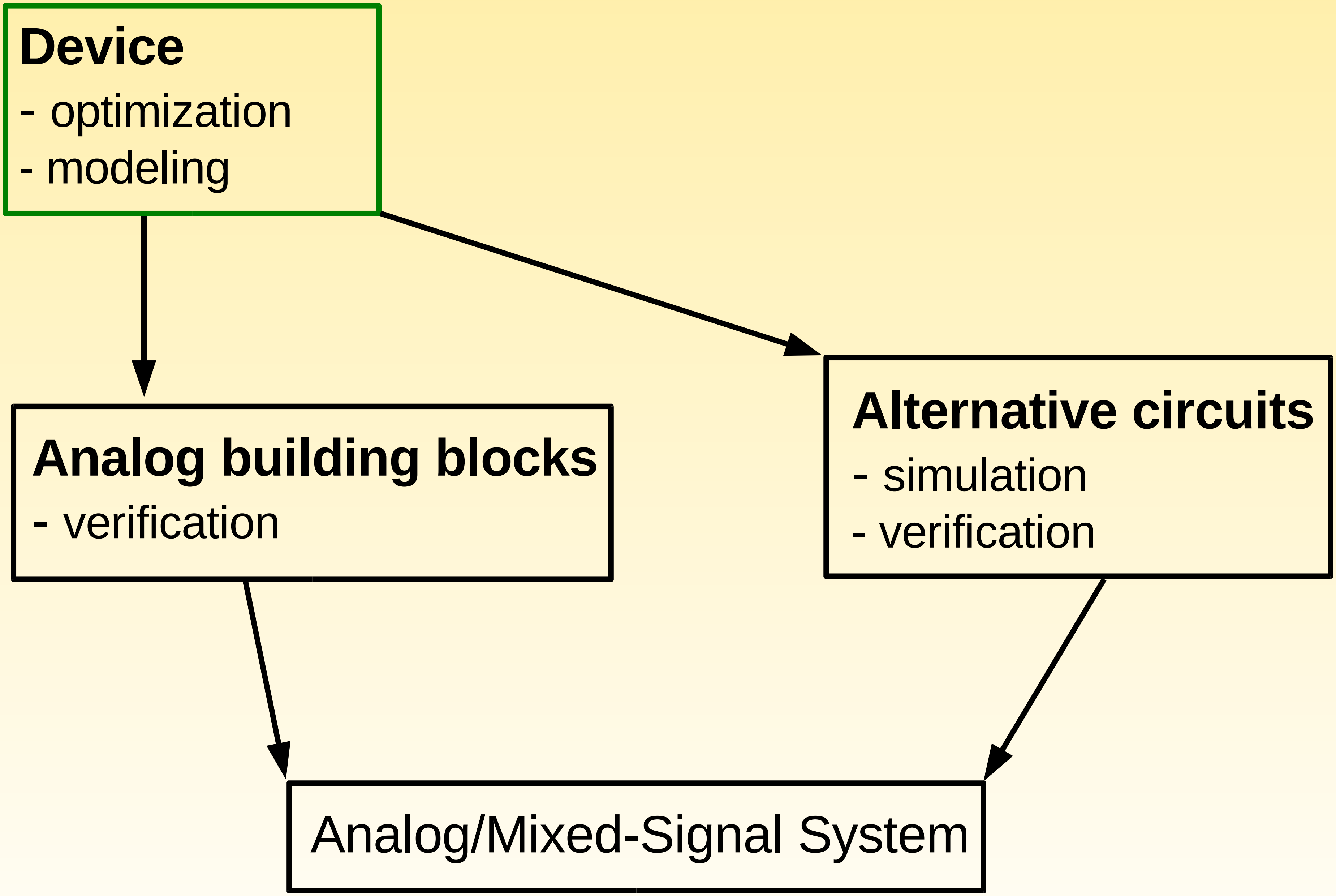
- Differential input stage, based on dual-V_T low voltage current mirror
- Fully differential OTA proposed
  - Simulation in 90nm CMOS ($\Delta V_T \approx 100$mV, V_{DD} = 0.6V, P=90µW)
  - Voltage gain: 37dB
  - GBW: 100MHz



⇒ **Similar results with TFETs possible ($\Delta V_T \approx$80mV)**

Conclusion

- **Device simulations and measurements show improved analog device properties**
  - Decreased short channel effects
  - Improved output conductance to current ratio (up to factor 2)
- **Calculations and SPICE simulations show benefits in analog circuit design**
  - Improved circuit properties
  - Additional degree of freedom in circuit design
  - Area savings by architectures with less transistor count
  - Alternative circuit design with dual-V_T


Device
- optimization
- modeling
Analog building blocks
- verification
Alternative circuits
- simulation
- verification
Analog/Mixed-Signal System

Vielen Dank!