

Y Transistors

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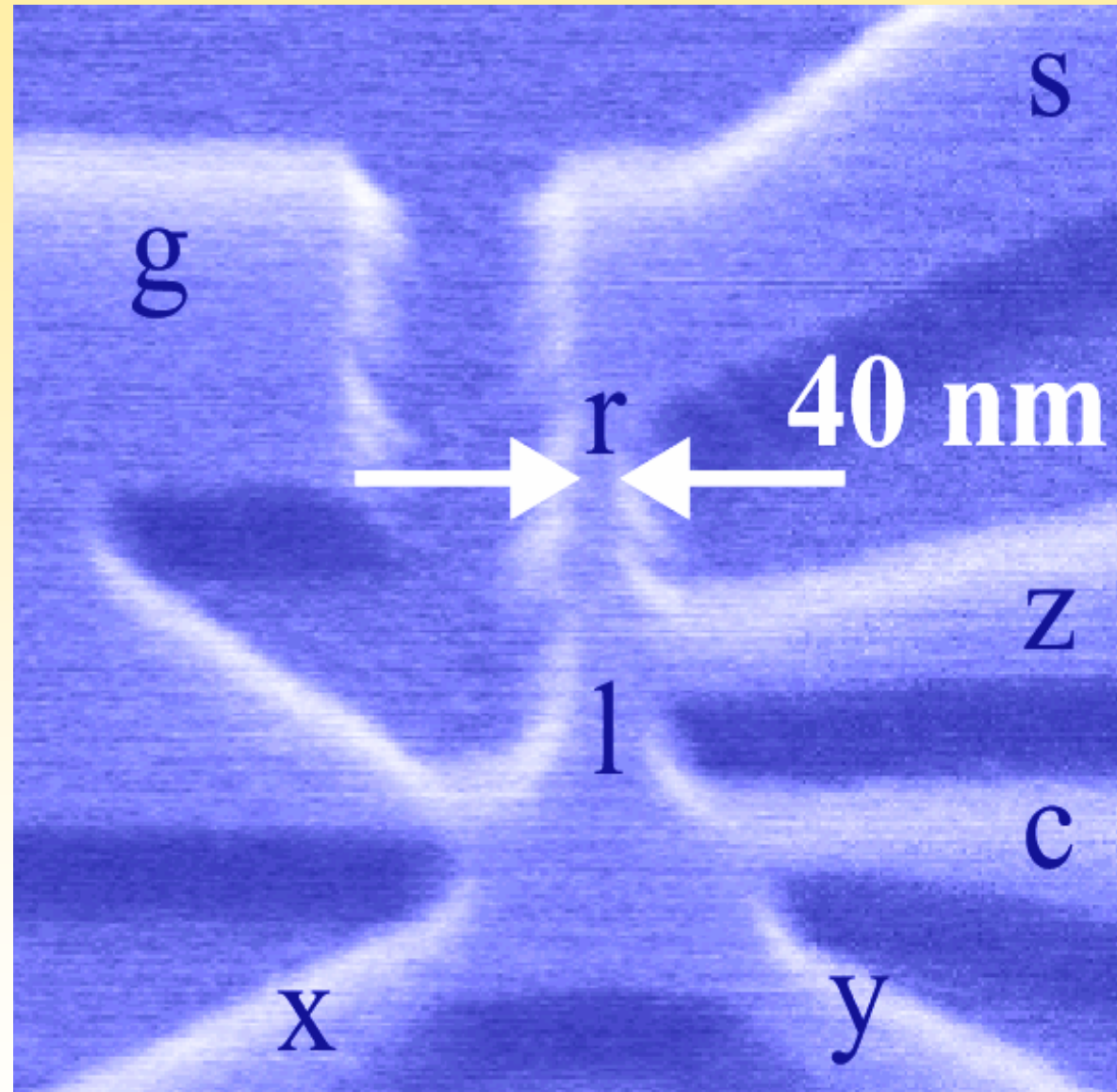
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Partner:

- Lehrstuhl für Technische Elektrophysik (TEP), TU München, Prof. Wachutka
- Lehrstuhl für Technische Elektronik (LTE), TU München, Prof. Schmitt-Landsiedel
- Infineon Technologies, München
- Nanoplus, Gerbrunn

OUTLINE

- Technology
- Gating
- Rectification
- Logics
- Counter



Micro to Nano: Entering the ballistic regime

- Development of Science and technology:

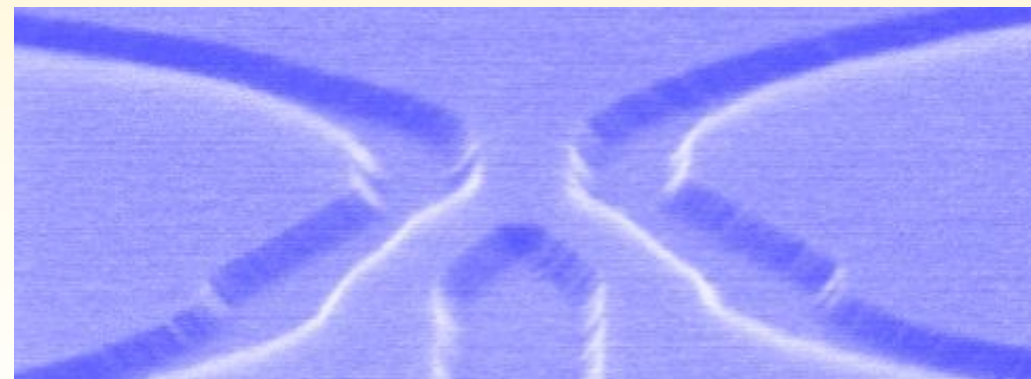
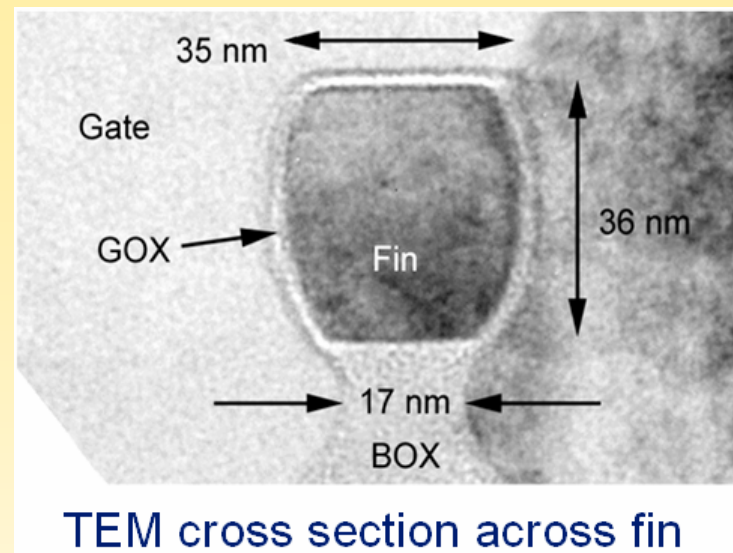
Ongoing miniaturisation

- ITRS 2004
- New transistor geometry:
z. B. FIN-FET

(picture from L. Risch, Infineon)

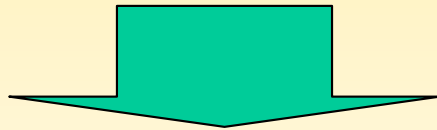
- New approach: Y-Nano-Transistors

- Ballistic switching in a lateral electric field
- FORNEL: room temperature operation
- Miniaturization below any scattering length

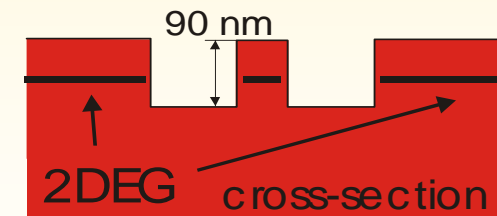
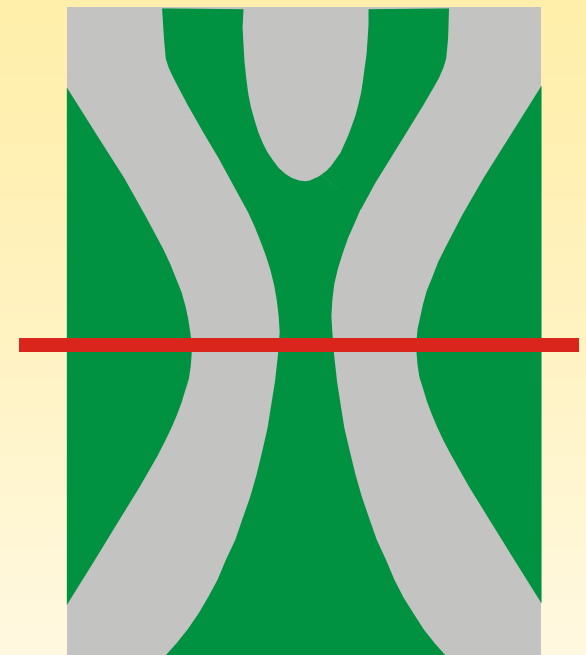


Lithography

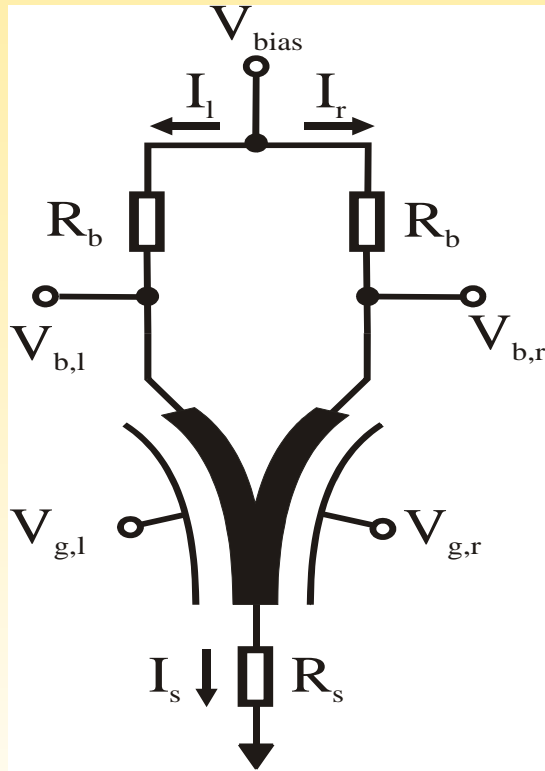
- Mask definition: electron beam lithography @ 100keV
- Lift-Off
- Wet-chemical etching



Nanostructure + side-gates

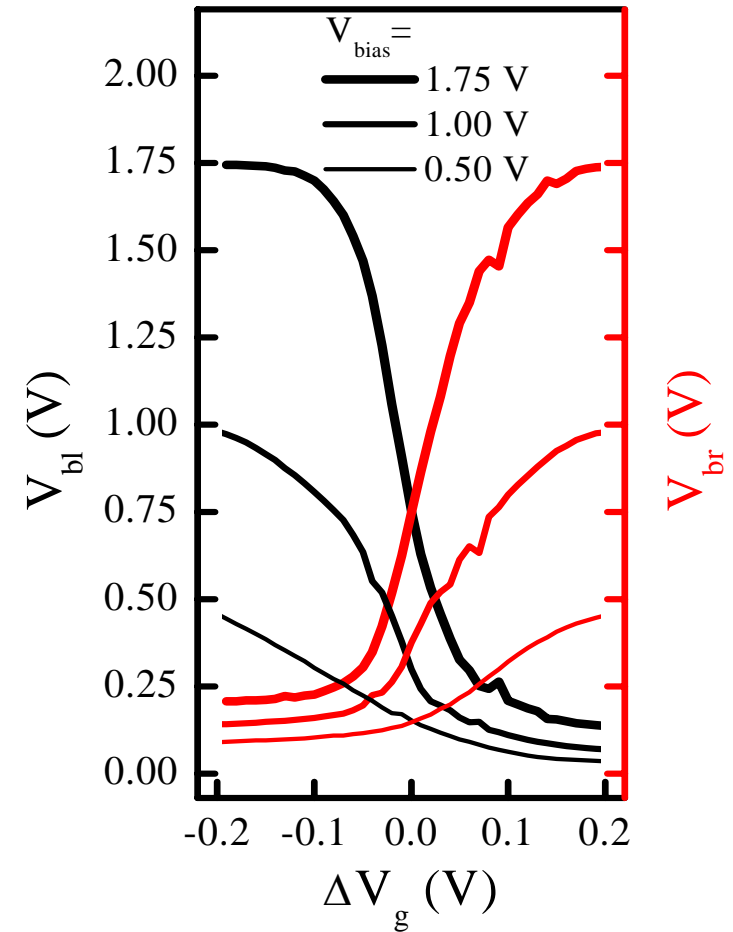


Y transistor: Switching between the branches



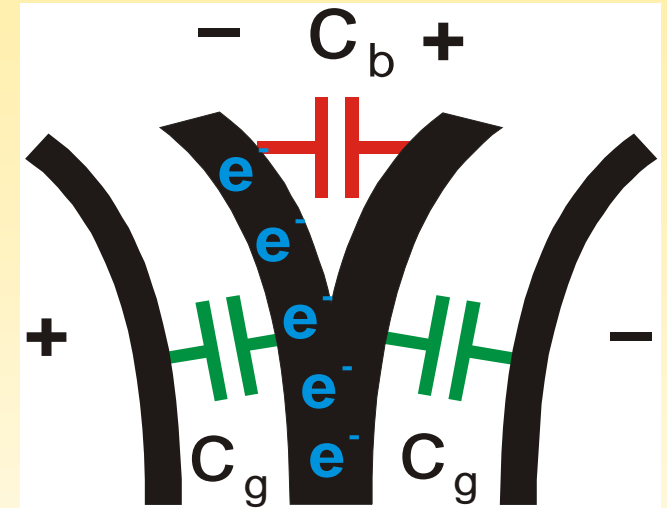
□ Push-pull Modus:

$$V_{gl} + V_{gr} = \text{const} \quad (dV_{gl} = -dV_{gr})$$



Additional capacitance

- Current conservation ($I_s + I_l + I_r = 0$):
- Switching parameters:



$$\gamma_l = \tanh[(\eta_g (\Delta V_g - V_{wp}) + \eta_b \Delta V_b) / V_s]$$

$$\gamma_r = \tanh[(\eta_g (\Delta V_g + V_{wp}) + \eta_b \Delta V_b) / V_s]$$

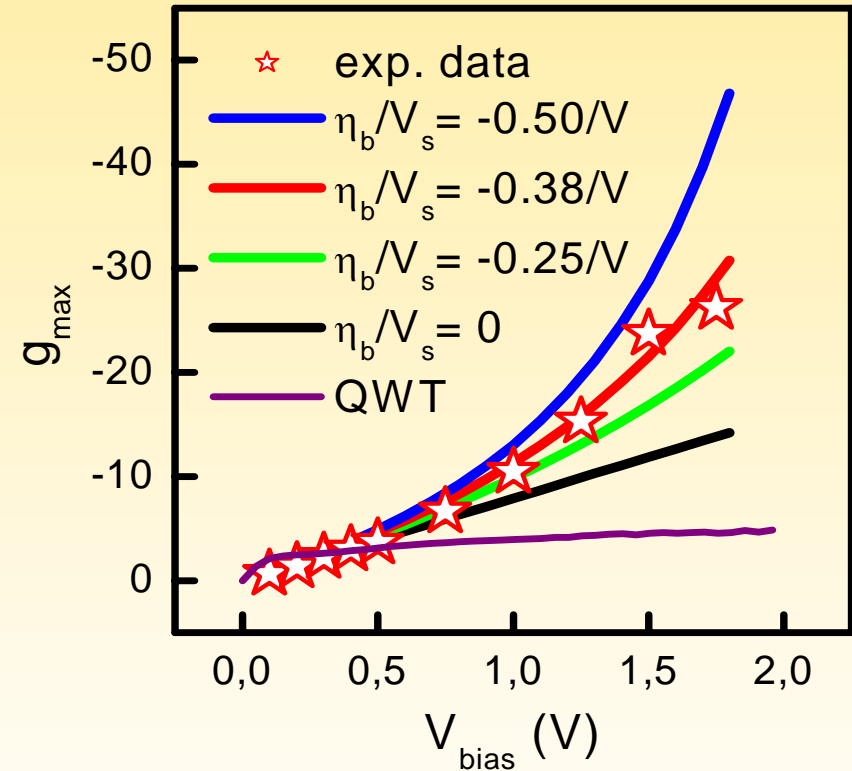
Superlinear increase of voltage gain

□ $g_{\max}(V_{\text{bias}})$ increases with the bias voltage

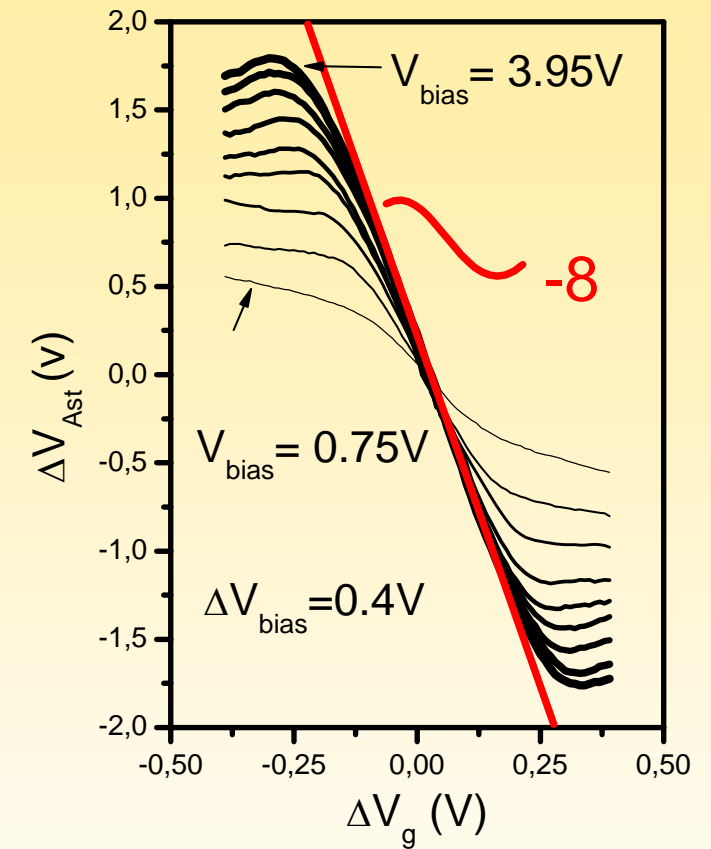
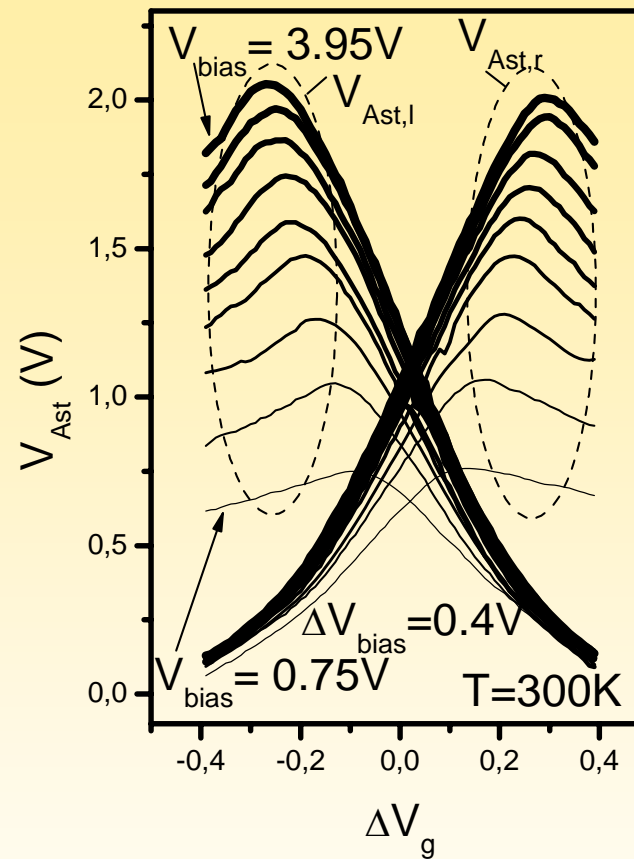
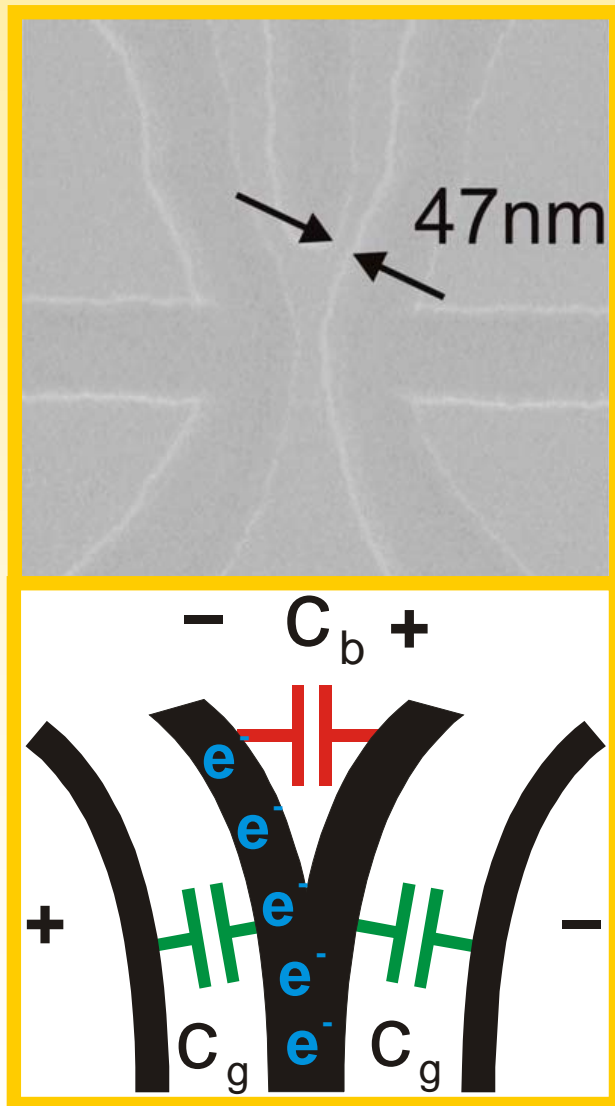
□ Analysis:

□ $\eta_b/V_s = 0$ linear

□ $\eta_b/V_s < 0$: non-linear $g_{\max}(V_{\text{bias}})$

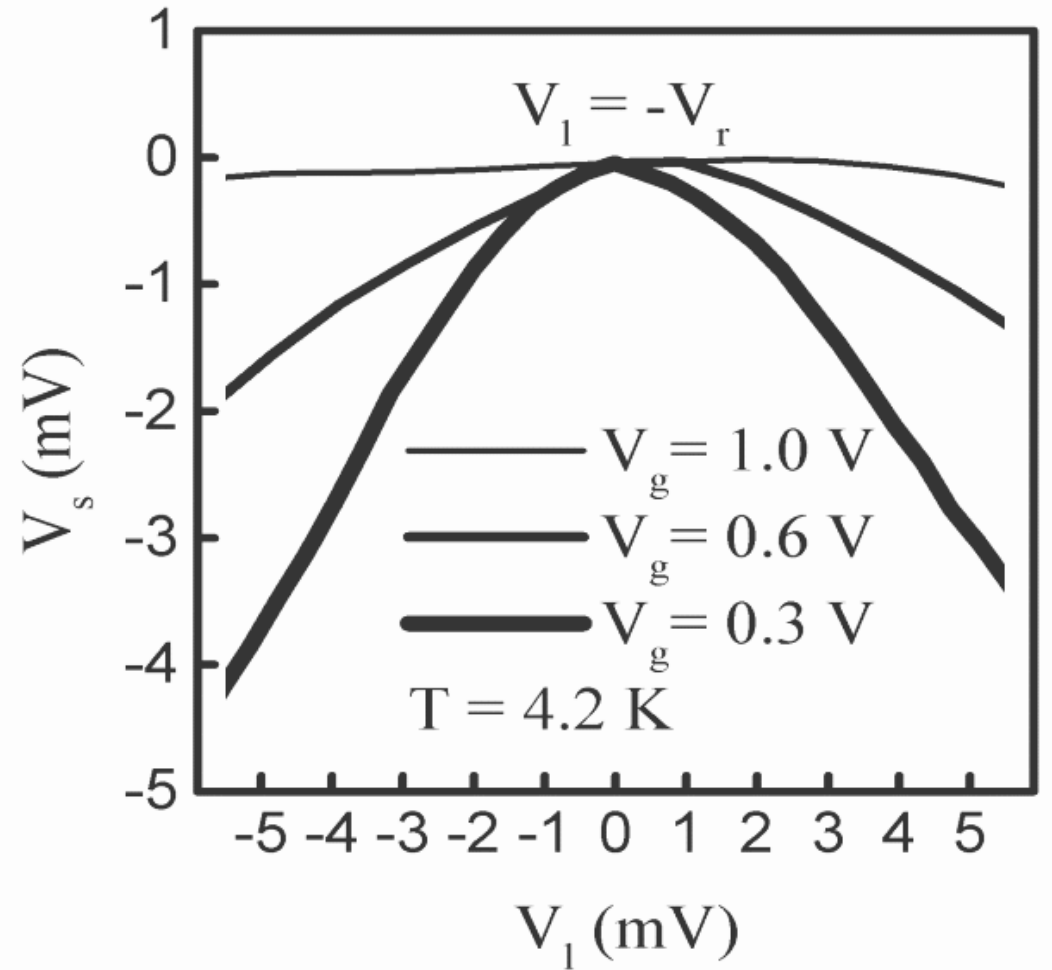
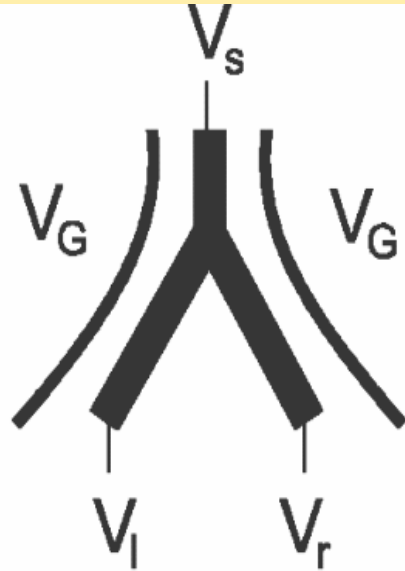
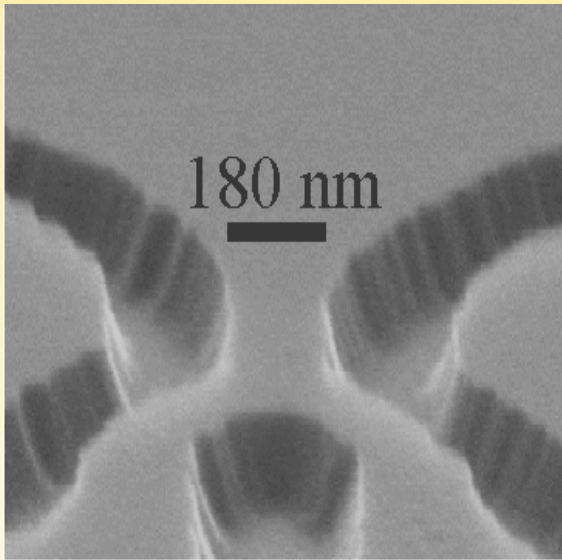


Selfgating at room temperature



- Electrochemical capacitance between the branches is dependent on the electrochemical potential. (M. Büttiker)

Higher functionality: Rectification

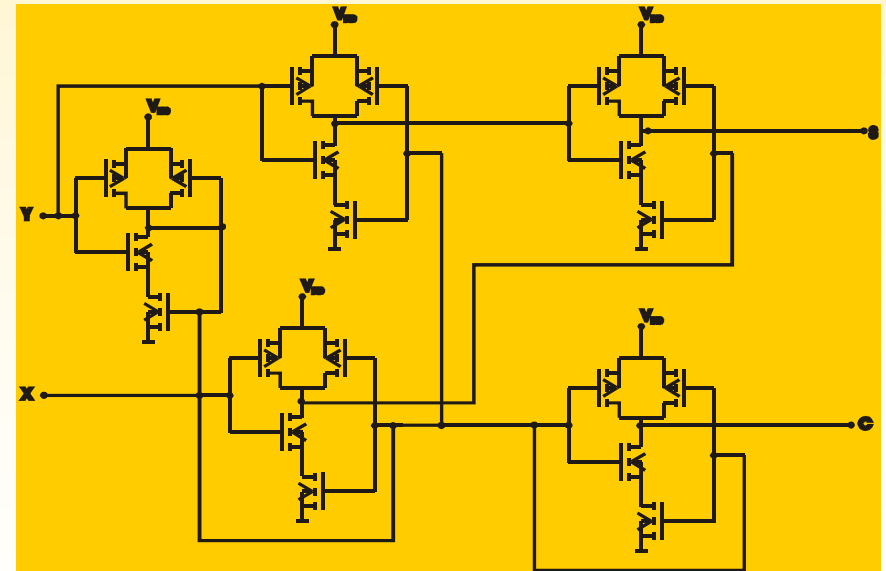


Processing of logic signals via gates: AND, XOR etc.

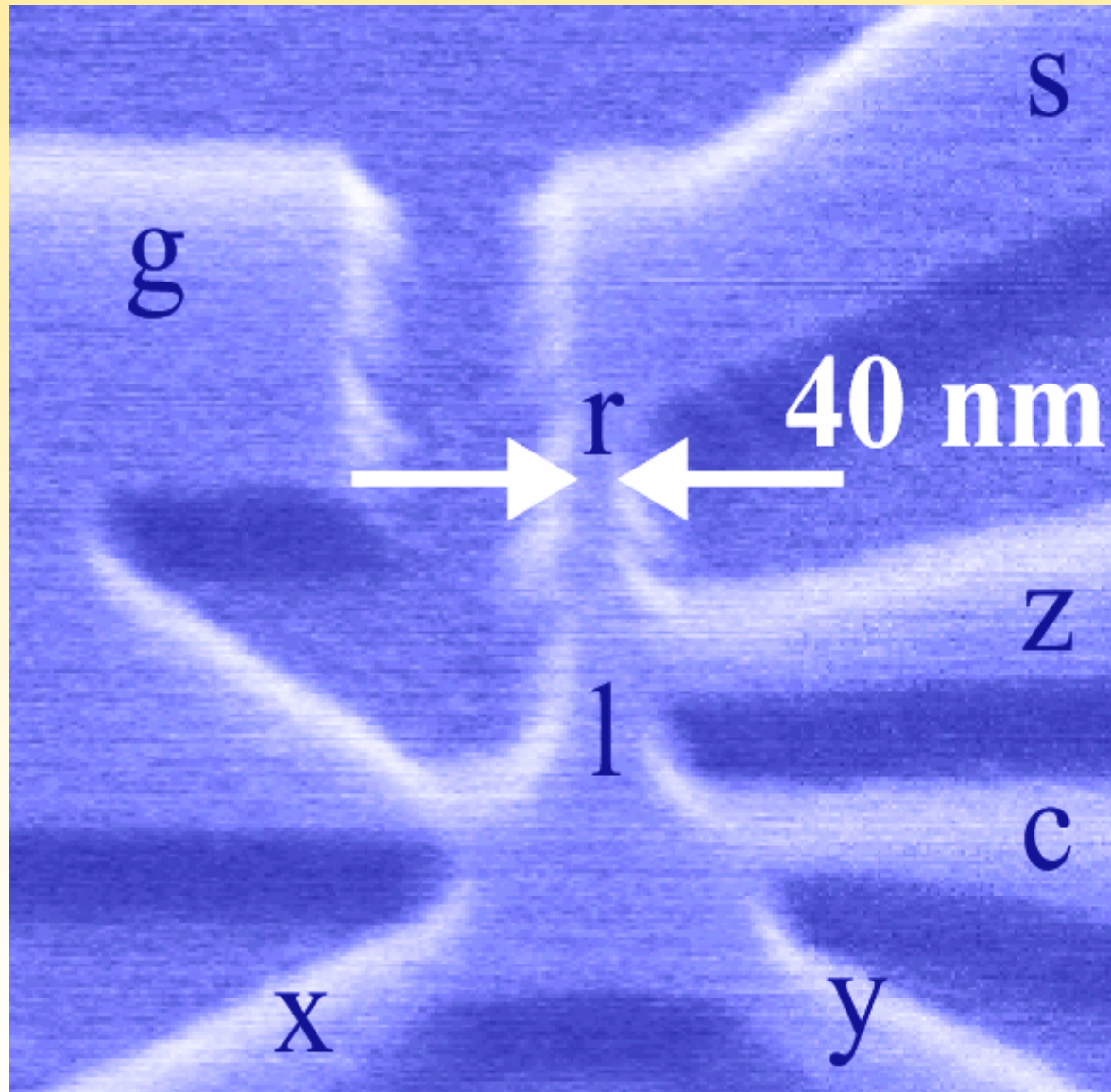
$$\begin{array}{r}
 2^1 \ 2^0 \\
 0 \ 0 \\
 + \ 0 \ 0 \\
 \hline
 0 \ 0
 \end{array}
 \quad
 \begin{array}{r}
 2^1 \ 2^0 \\
 0 \ 1 \\
 + \ 0 \ 0 \\
 \hline
 0 \ 1
 \end{array}
 \quad
 \begin{array}{r}
 2^1 \ 2^0 \\
 0 \ 0 \\
 + \ 0 \ 1 \\
 \hline
 0 \ 1
 \end{array}
 \quad
 \begin{array}{r}
 2^1 \ 2^0 \\
 0 \ 1 \\
 + \ 0 \ 1 \\
 \hline
 1 \ 0
 \end{array}$$

X_i	Y_i	XOR	AND
1	1	0	1
0	1	1	0
1	0	1	0
0	0	0	0

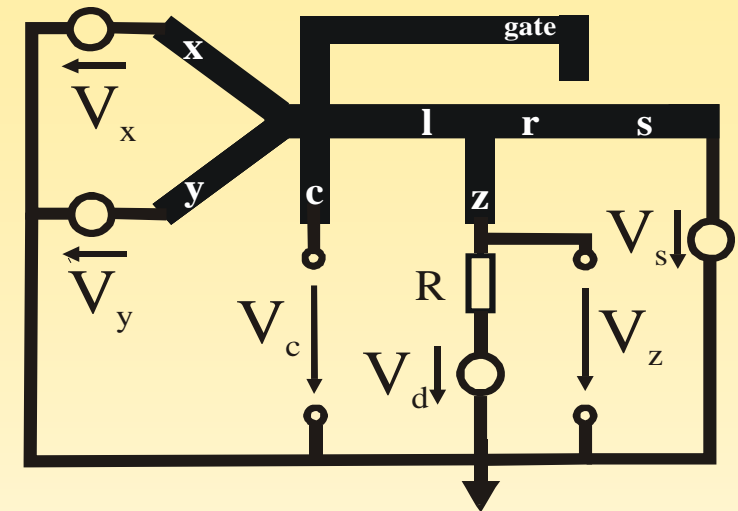
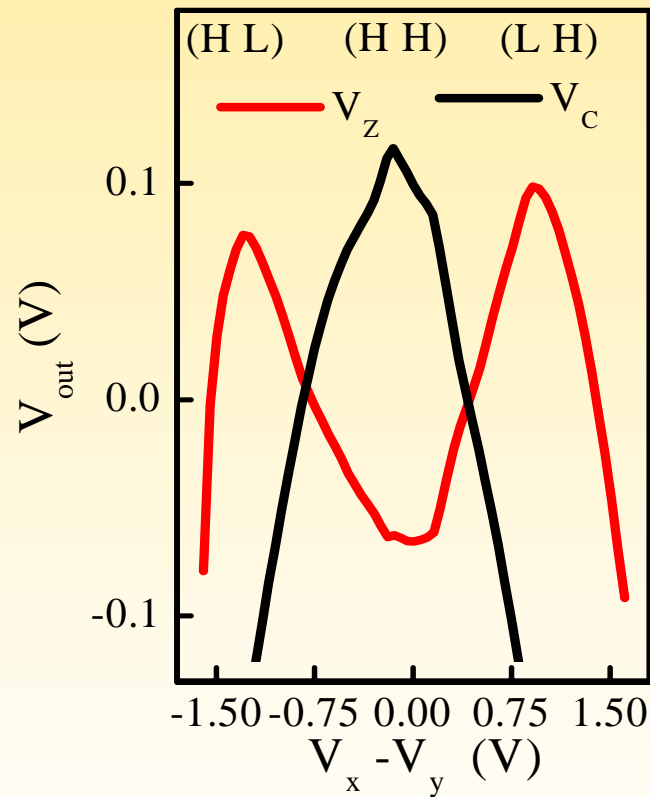
halfadder



Logic Gates and Simple Computing

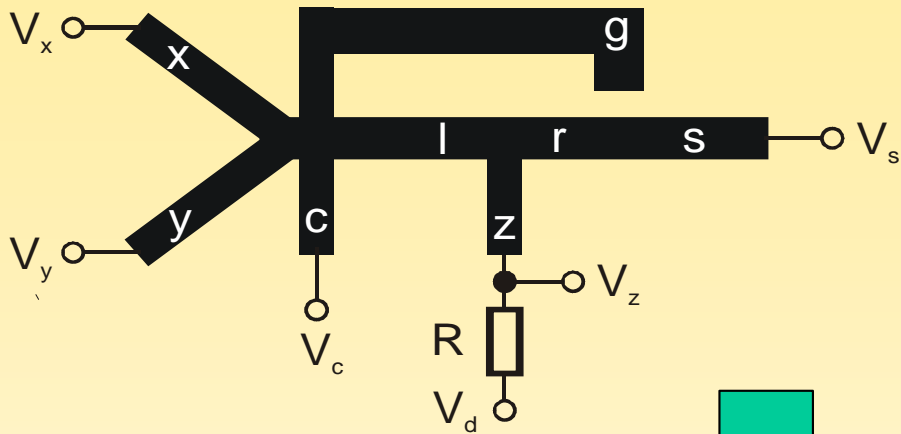


Half adder function



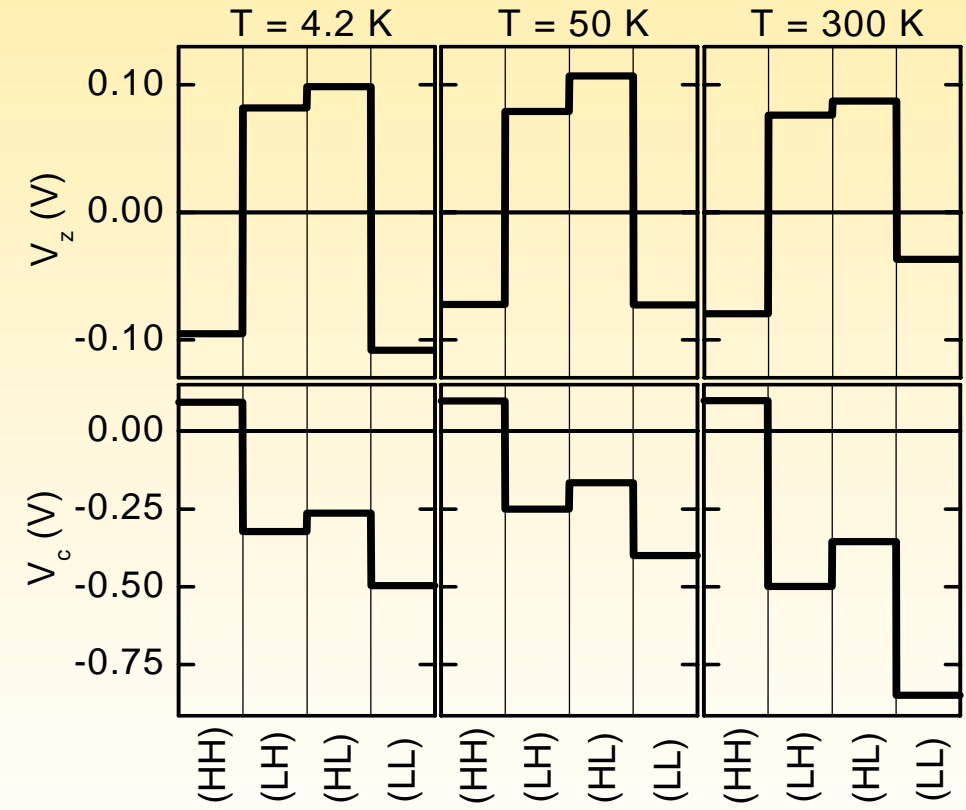
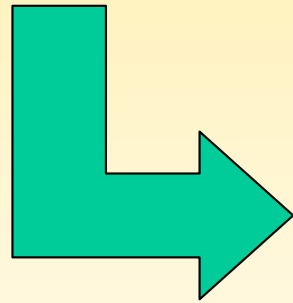
- Push-Pull-Mode:
 $V_x + V_y = 0.3 \text{ V}$
- Rectification: $V_c < (V_x + V_y)/2$
- Self induced Switching:
M-shaped V_z -characteristic

Half adder at RT



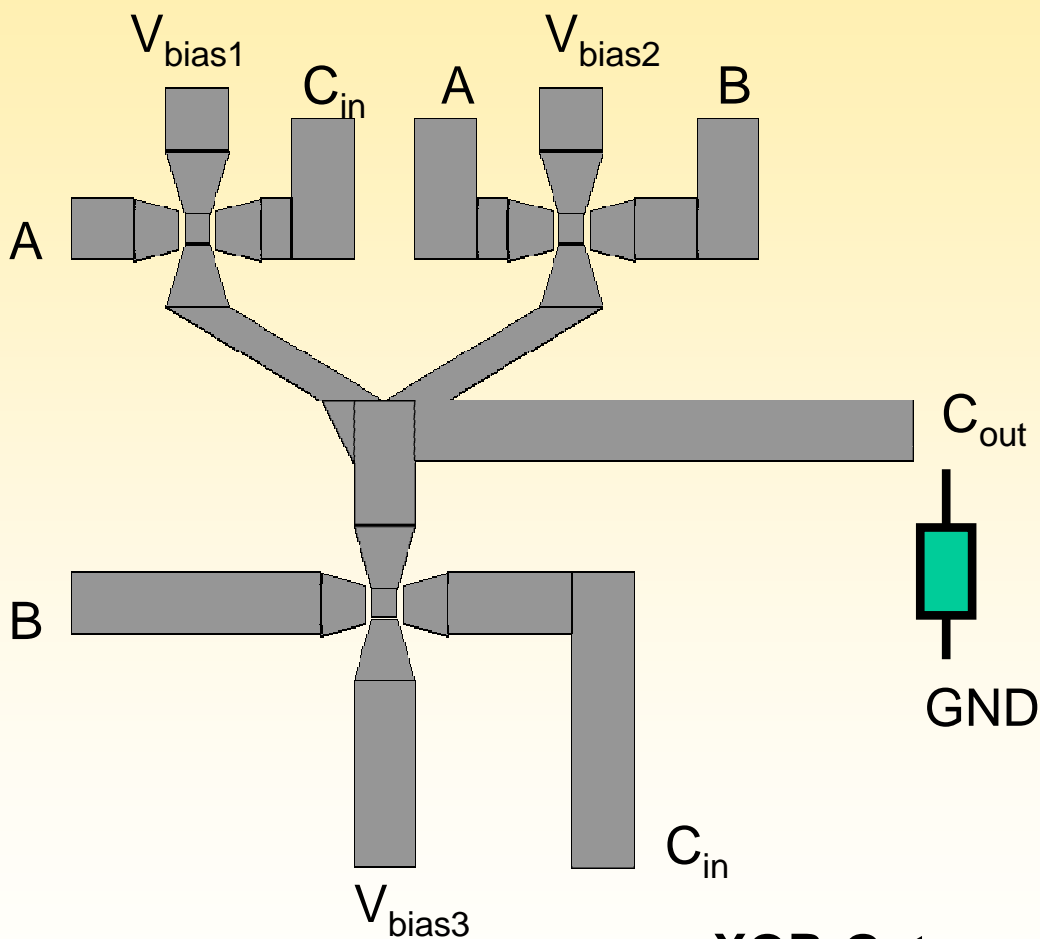
Demonstration of Logic at RT:

X	Y	Z	C
H	H	L	H
H	L	H	L
L	H	H	L
L	L	L	L

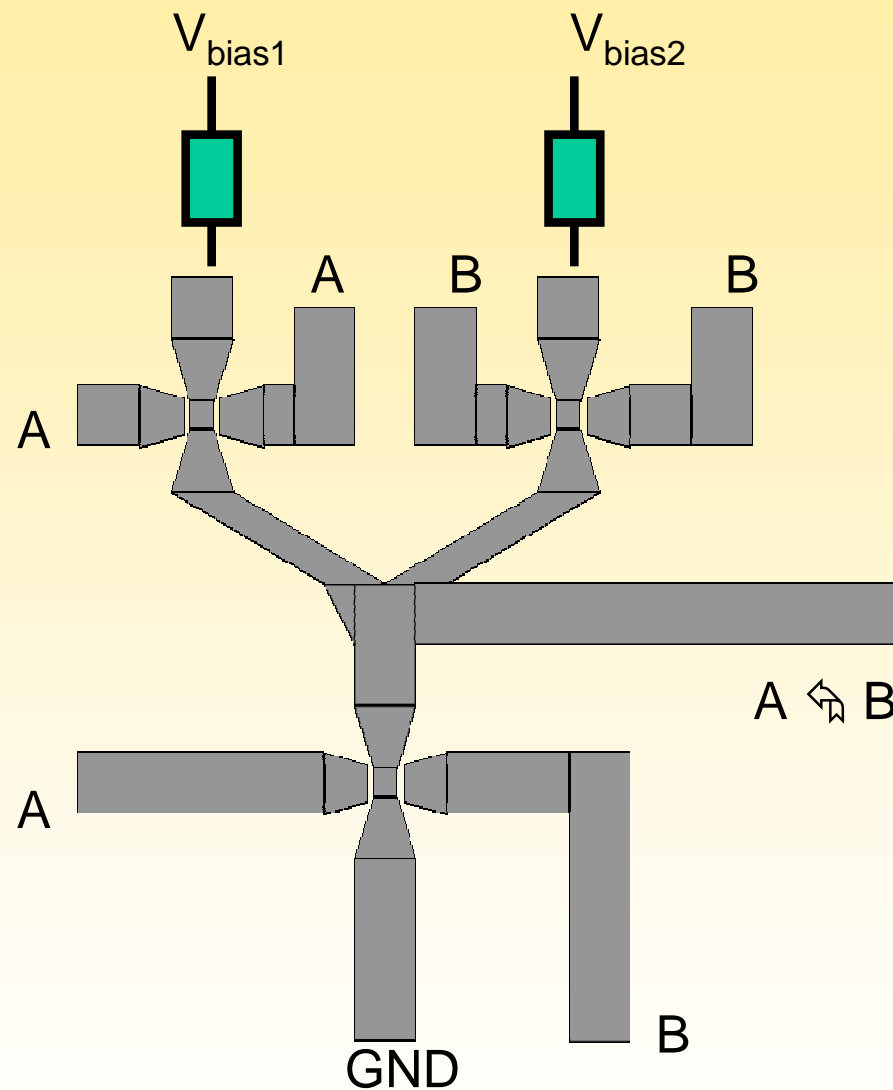


Logische Eingangspegel (XY)

Y-Transistor: more logics & full adder

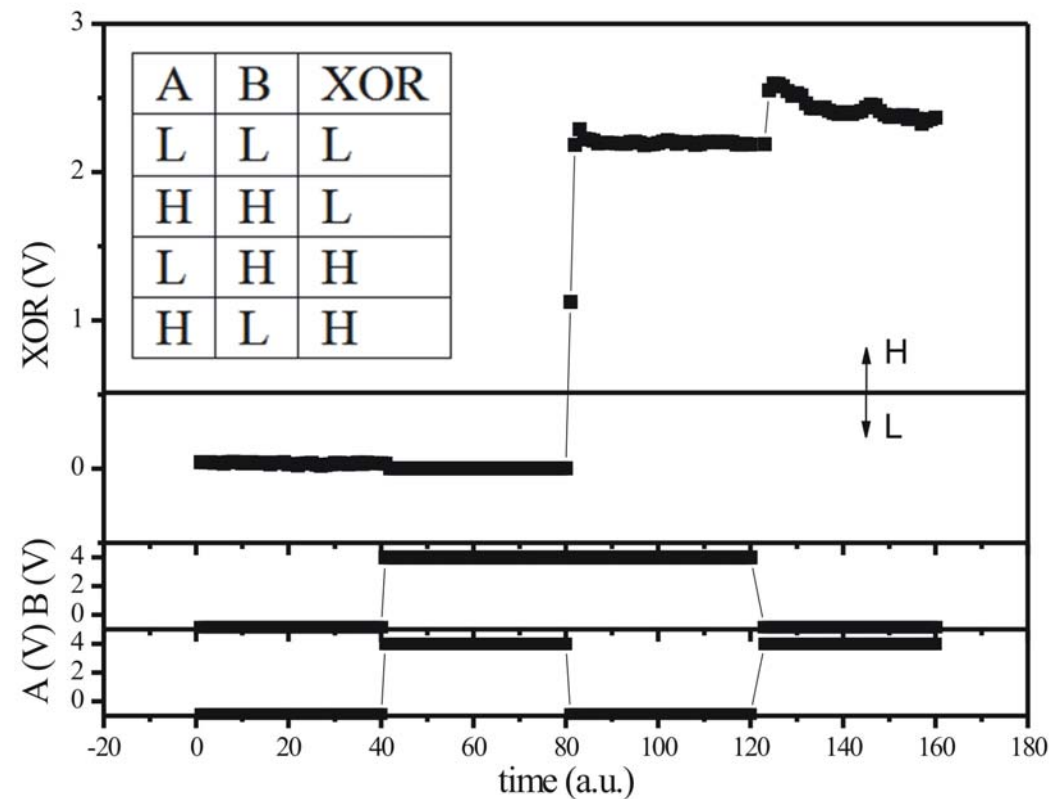
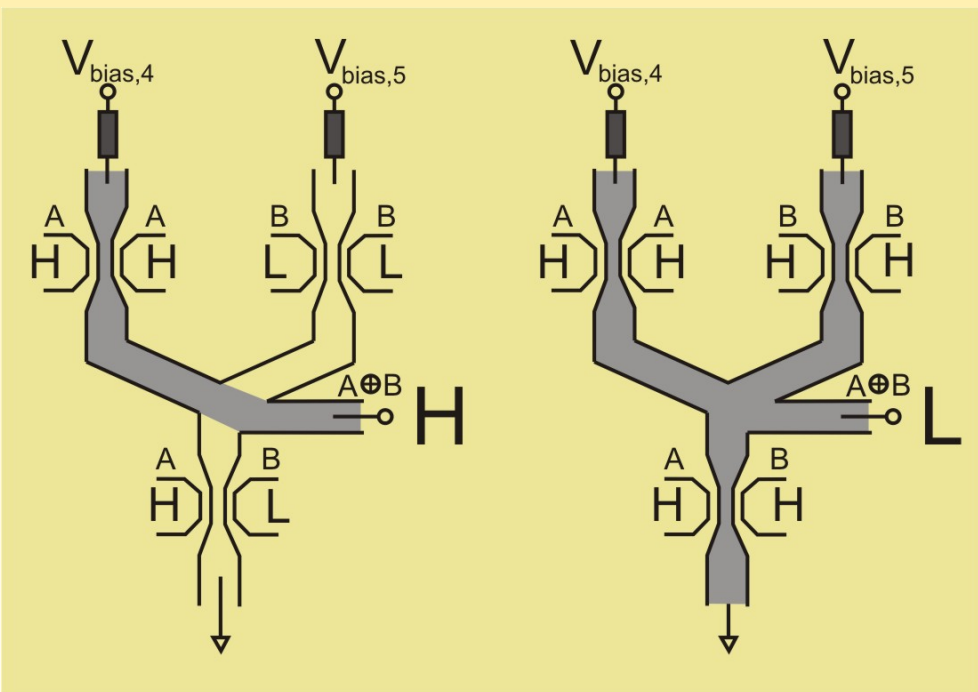


XOR-Gate

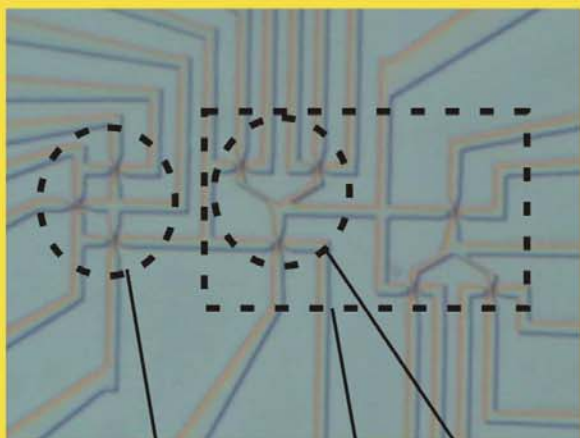


Carry-Bit

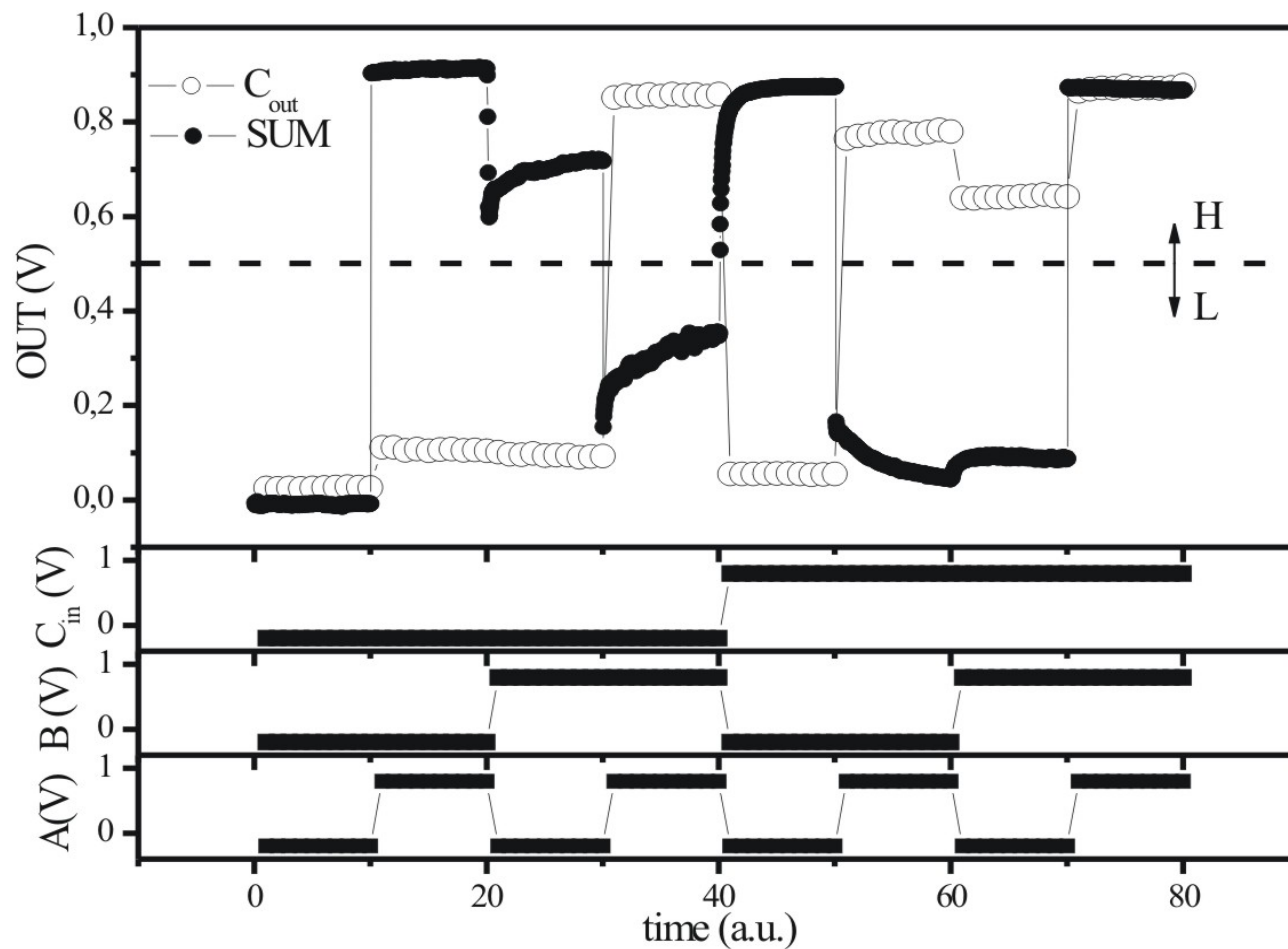
XOR-Gate at RT



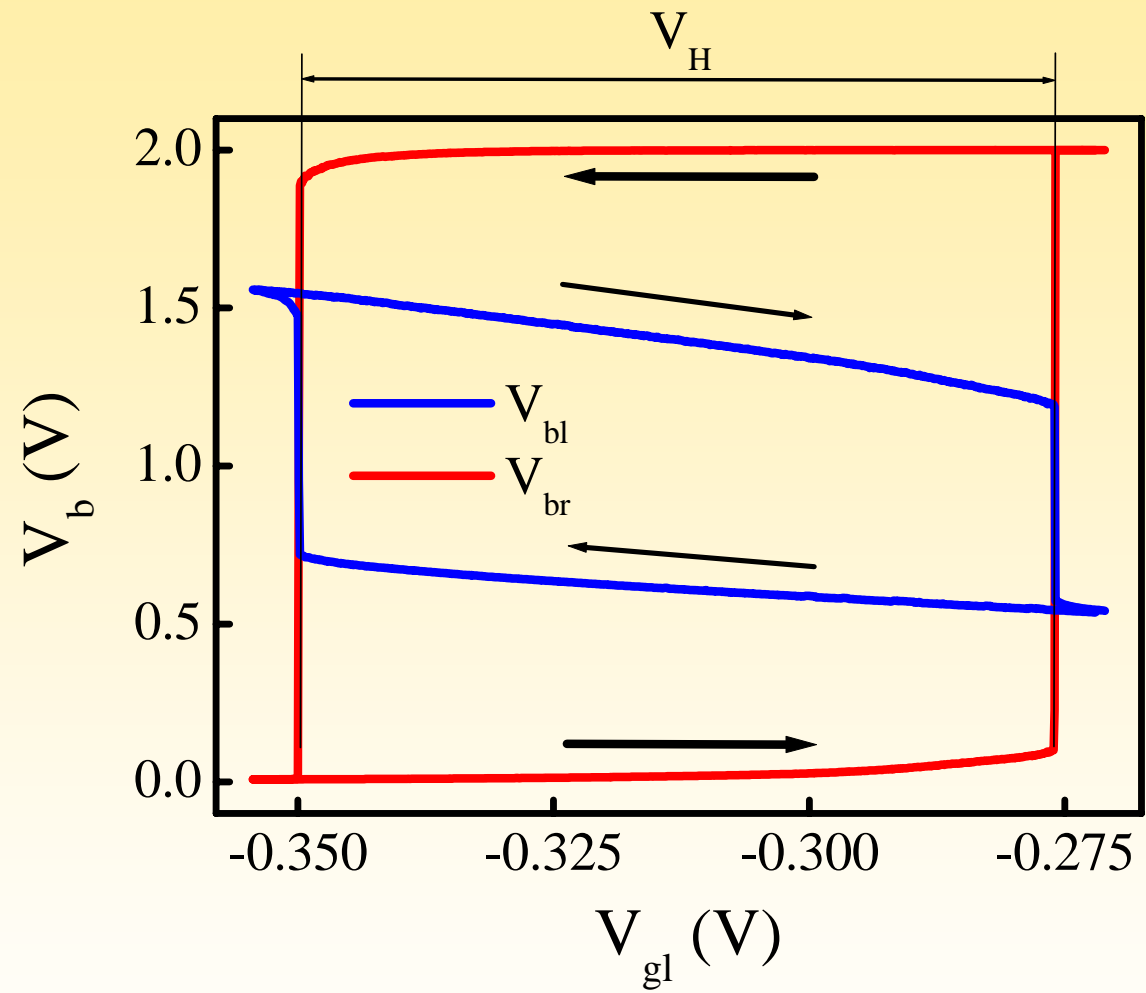
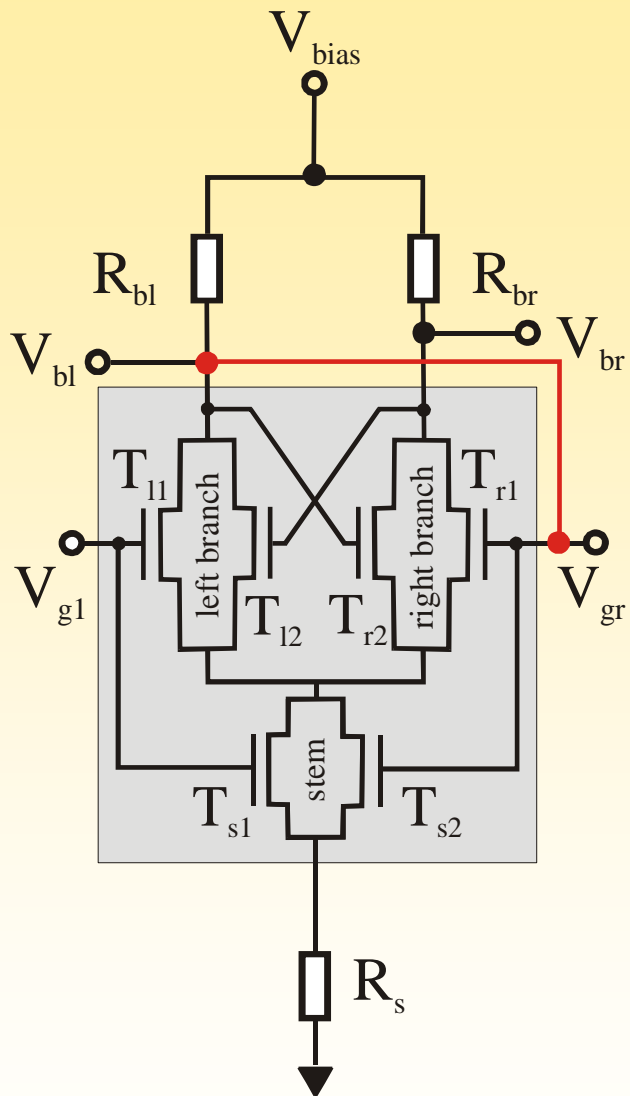
Fulladder at RT



Carry bit device
XOR-gate
SUM bit device

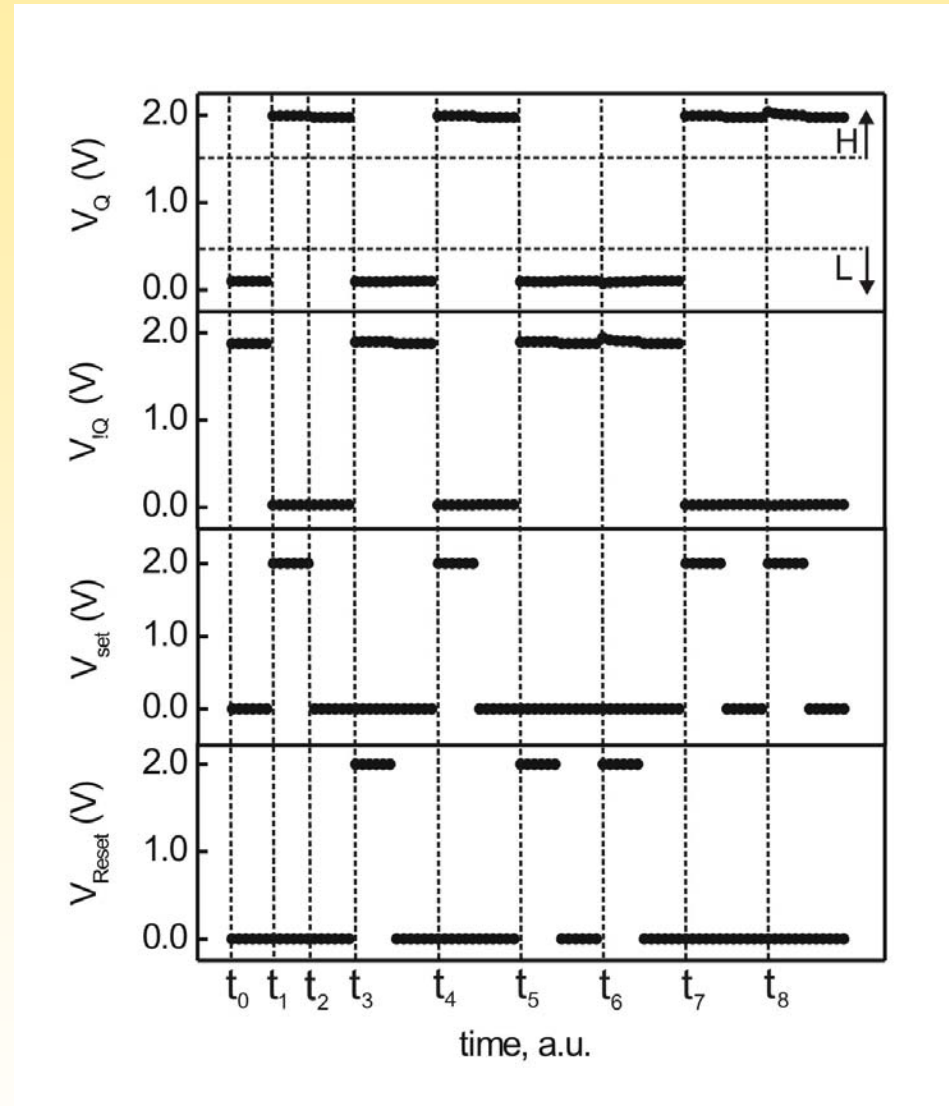


Bistable Mechanism: Feedback



Reitzenstein et al., Appl. Phys. Lett., 2003

RS-FlipFlop



D. Hartmann et al., Electron. Lett., 2005, 41, pp. 303-304

Summary

- Gain in Y-transistors at room temperature
- Logics, Adders

Acknowledgement

- Our partners in FORNEL
- Bayerische Forschungsstiftung



Many thanks for your attention!