



Simulation of the Silicon Tunnel FET

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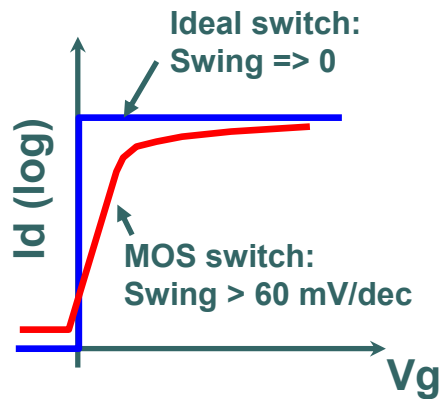
Outline

- Motivation
- Device structure and operation
- Subthreshold swing
- Optimizing the dielectric and the silicon thickness
- 2D cross-sections
- Conclusion

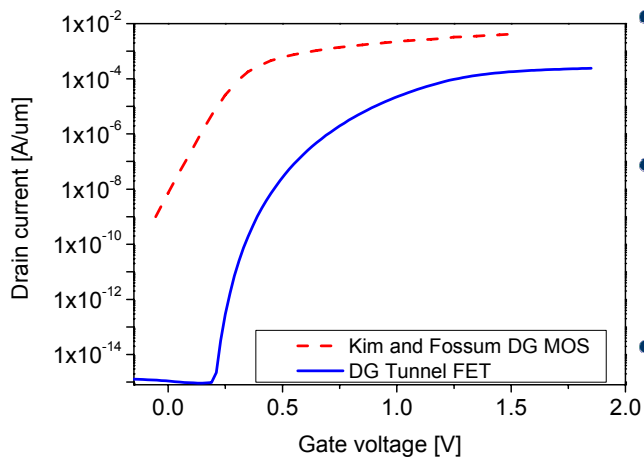


Tunnel FET as solution to MOSFET limitations

- The **subthreshold swing** of a MOSFET is limited by its physics (formation of inversion channel determines swing)
 - Tunnel FETs use different physics and can have Swing < 60 mV/dec.
- As MOSFETs become smaller, **off-current** increases due to leakage
 - Tunnel FETs have energy barrier in OFF-state which avoids this power-consuming leakage.

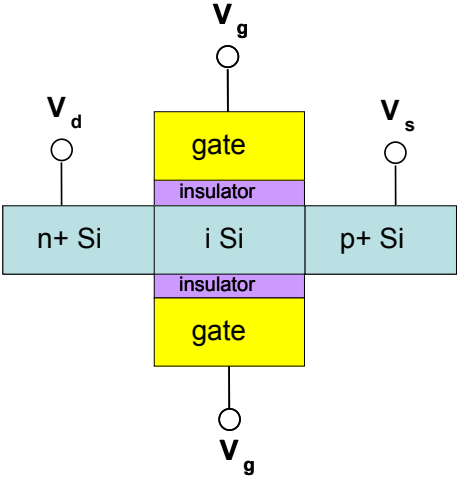


Comparison: DG Tunnel FET and DG MOSFET



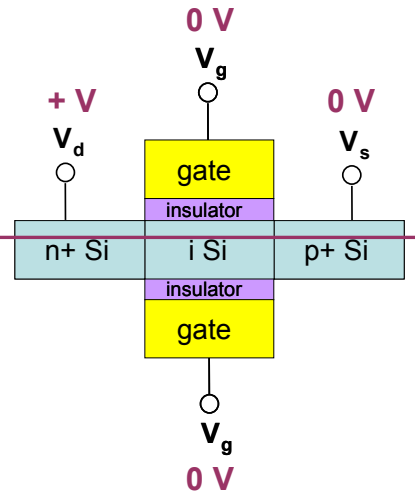
- Same dimensions (t_{Si} , t_{ox} , channel / i-region length).
- Tunnel FET swing much steeper closer to off-state.
- I_{off} much lower for Tunnel FET.

Device structure



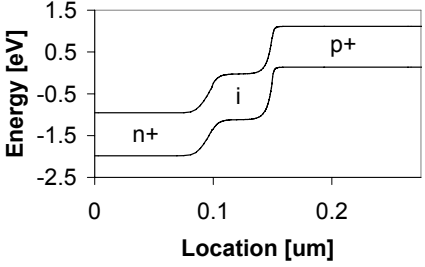
- n+ terminal = "drain"
- p+ terminal = "source"
- Insulator:
 - SiO₂ or
 - High-K
- Metal gates

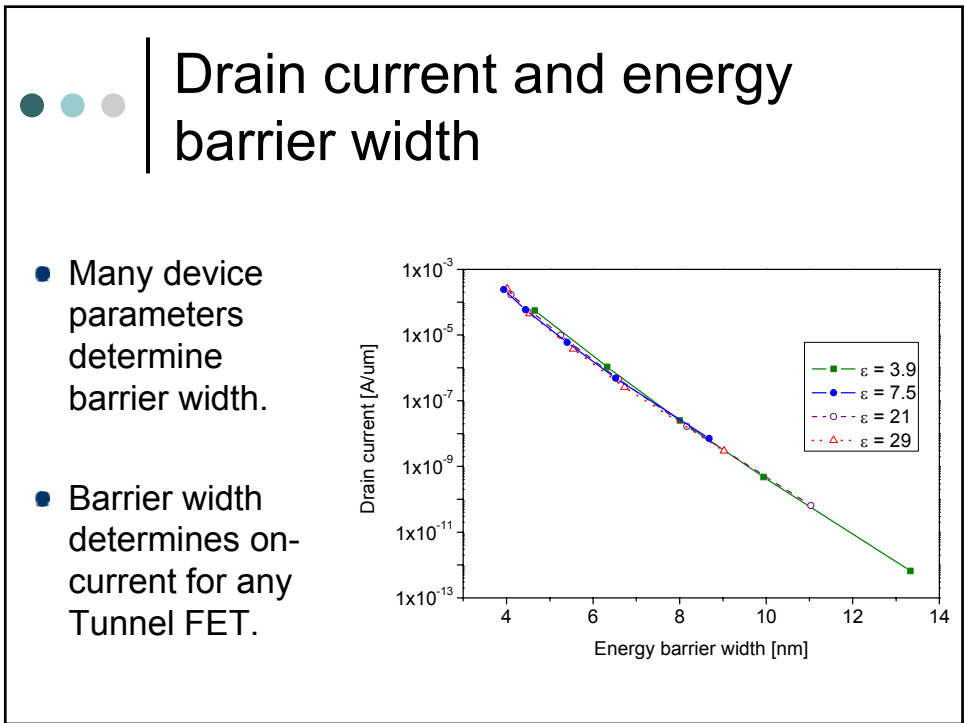
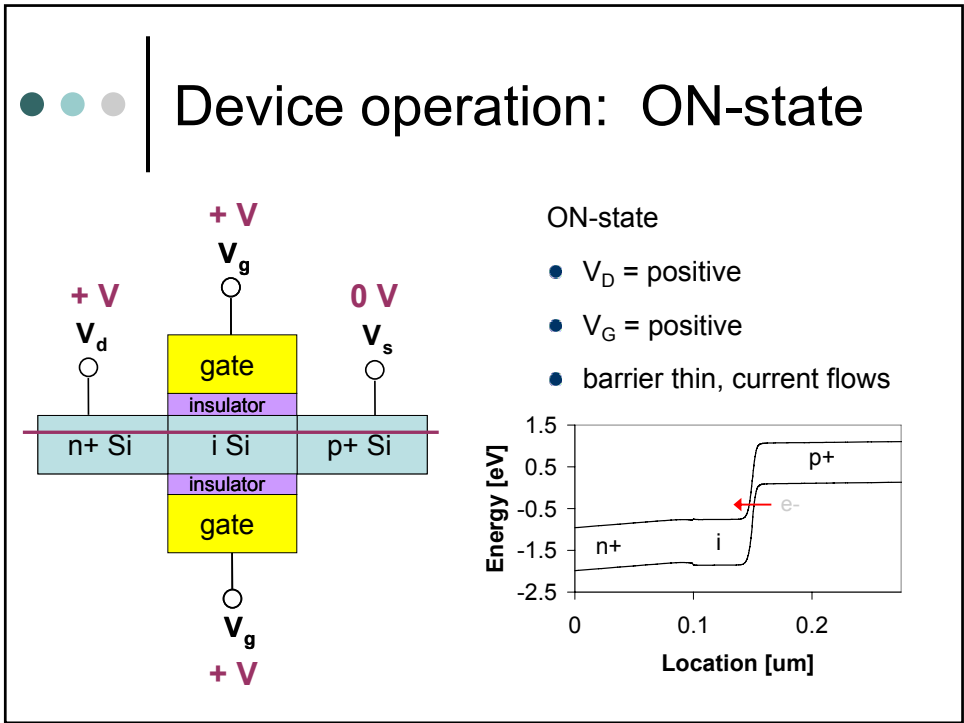
Device operation: OFF-state



OFF-state

- V_D = positive
- V_G = 0
- no current flows







Subthreshold swing

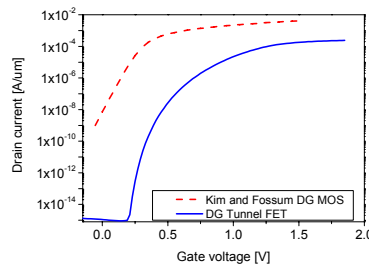
- In general,
$$S = \frac{dV_g}{d(\log I_d)} [mV / dec]$$
- For a MOSFET,
$$S_{MOSFET} = \ln(10) \frac{kT}{q} \left(1 + \frac{C_d + C_{it}}{C_{gate}}\right) [mV / dec]$$
- For a Tunnel FET,
$$S_{TFET} = \frac{V_{gs}^2}{5.75(V_{gs} + Const)} [mV / dec]$$



Tunnel FET subthreshold swing

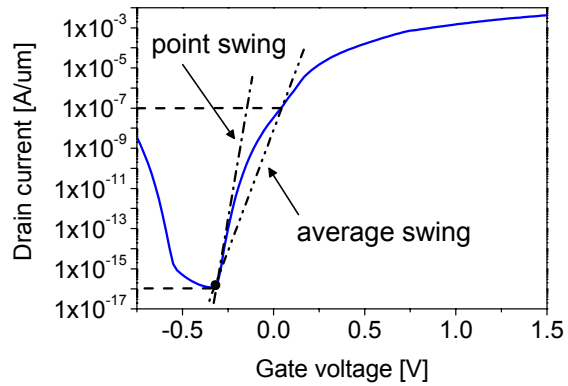
$$S_{TFET} = \frac{V_{gs}^2}{5.75(V_{gs} + Const)} [mV / dec]$$

- Dependence on V_{gs} :
 - Means that slope is not a straight line (on log scale) in subthreshold.
- Dependence on constant:
 - Includes drain doping, gate dielectric constant, tunnel junction abruptness, etc.

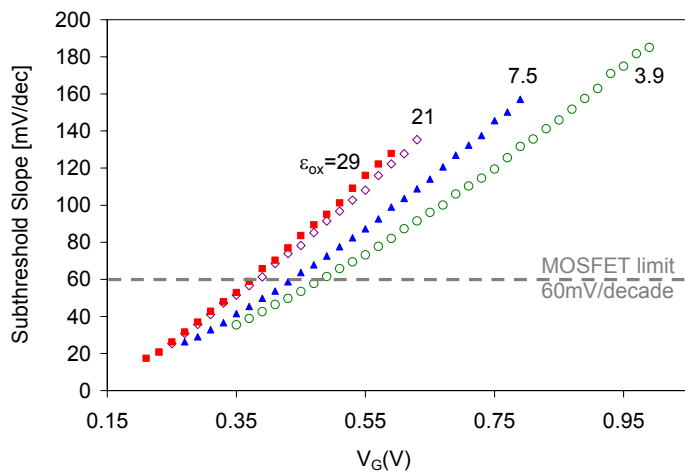


Swing definitions

- Point swing: lowest value of swing on I_d - V_g curve.
- Average swing: swing as device turns on, up until threshold voltage.



Swing and gate voltage



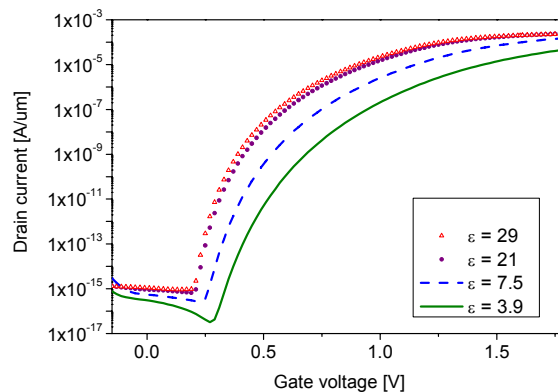
- Unlike MOSFET, Tunnel FET's subthreshold swing is a function of V_G .
- High-K dielectrics attain low swing values at low V_G .

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Improved characteristics with high-K dielectric

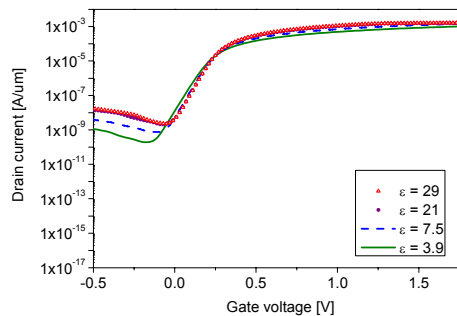
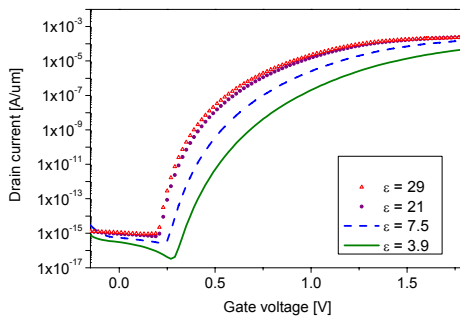
- Higher dielectric constant gives
 - higher on-current
 - steeper S
- Benefits from high-K saturate with ϵ value.
- Increase in on-current much more than for MOSFET.



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Tunnel FET vs. MOSFET with high-K dielectric



- On-current:
 - More improvement shown in Tunnel FET, due to improved coupling between gate and tunnel barrier.
- Subthreshold swing:
 - More improvement shown in Tunnel FET – swing of conventional MOSFET remains constant.

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Tunnel FET current and its proportionality to gate dielectric constant (1/2)

$$T(E) \propto \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g + \Delta\Phi)} \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{ox} t_{Si}}\right) \Delta\Phi \quad [1]$$

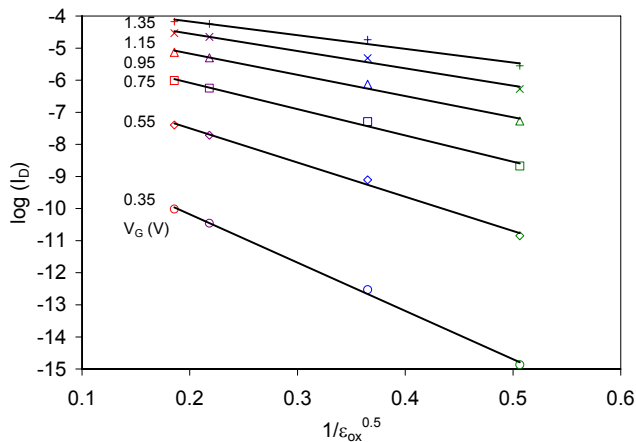
$$\log I_D \propto \left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g + \Delta\Phi)} \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{ox} t_{Si}}\right) \Delta\Phi$$

$$\log I_D \propto \sqrt{\frac{1}{\epsilon_{ox}}}$$

[1] J. Knoch and J. Appenzeller, DRC '05, 63rd, vol. 1, June 20-22, 2005, pp. 153-156.



Tunnel FET current and its proportionality to gate dielectric constant (2/2)



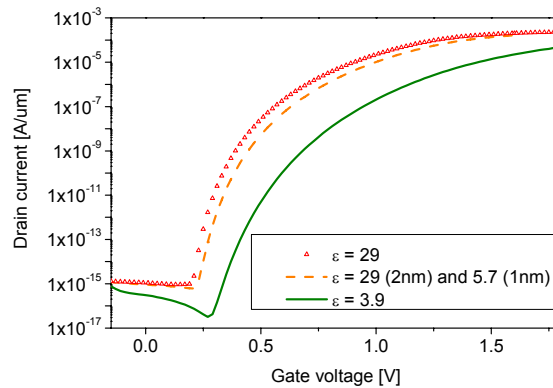
- Proportionality between $\log(I_D)$ and $1/\epsilon_{ox}^{0.5}$ seen over a range of gate voltages.

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Compatibility with conventional MOSFET fabrication: the interfacial layer

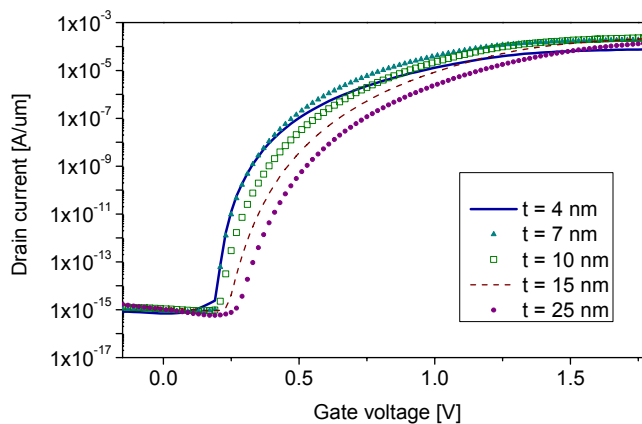
- The dielectric materials studied here: HfO_2 and ZrO_2 , typically have an interfacial layer which improves interface with Si.
- For Tunnel FET, this is almost as good as high-K dielectric alone.



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Optimization of the Si body thickness of the DG Tunnel FET

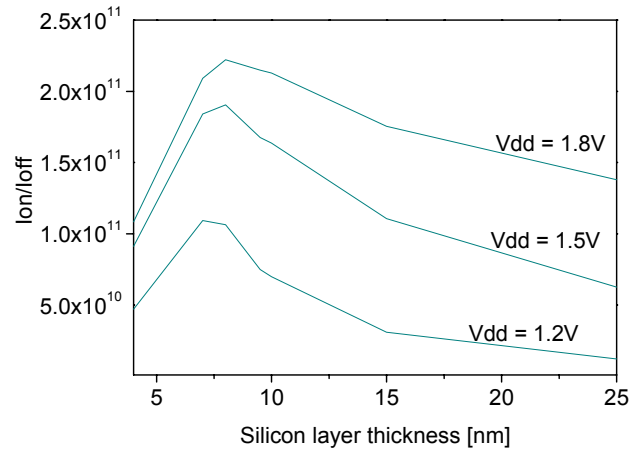


- I_{off} almost constant with Si thickness.
- I_{on} decreases when $t_{\text{Si}} < 10$ nm.
- Therefore, optimum t_{Si} gives best $I_{\text{on}}/I_{\text{off}}$.
- Subthreshold swing improves with thinner Si.

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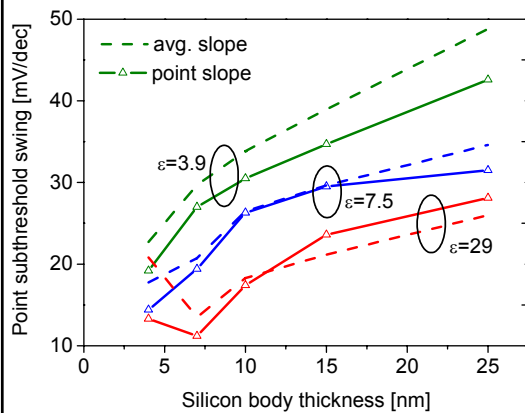
I_{on}/I_{off} ratio vs. Si body thickness of DG Tunnel FET

- Optimum silicon layer thickness exists.
- Exact value will depend on device dimensions and V_{DD}.
- Here, t_{Si,opt} ~ 7-9 nm.



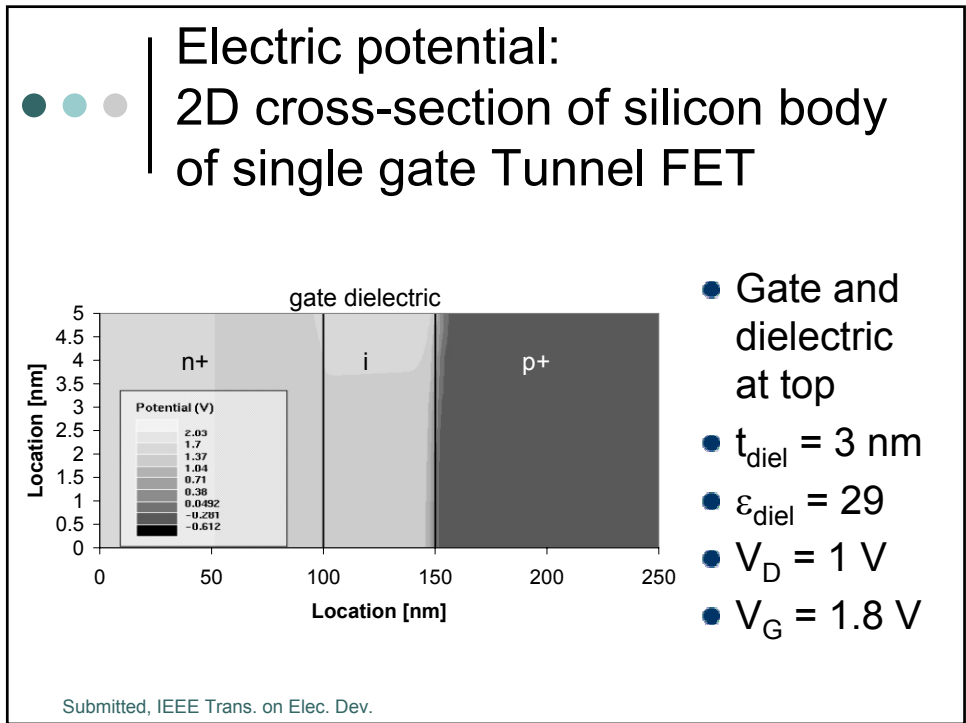
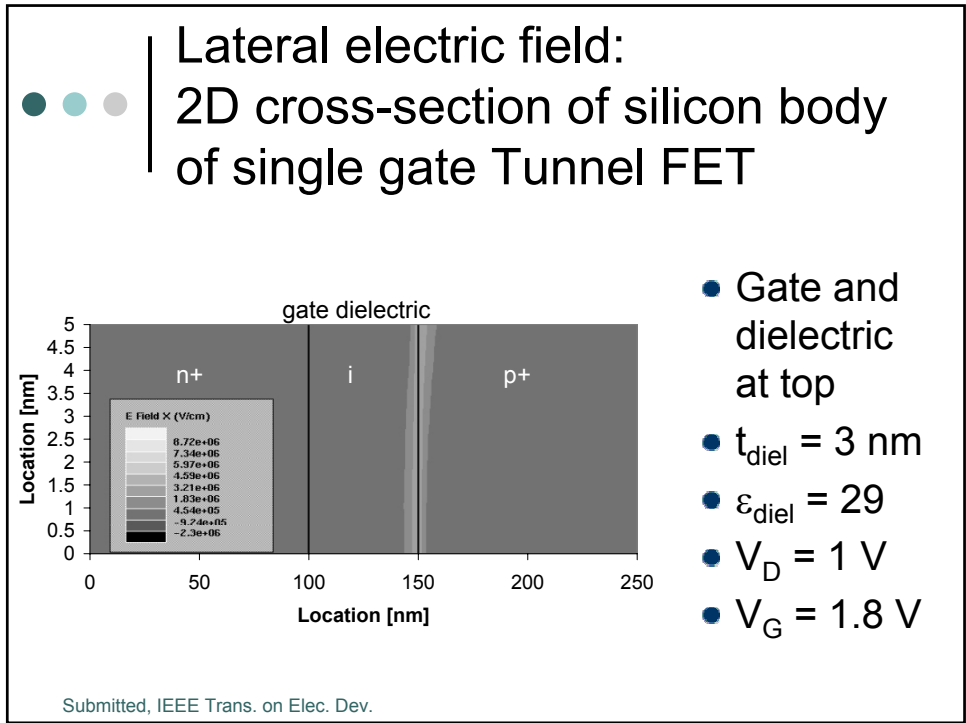
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Subthreshold swing vs. Si body thickness of DG Tunnel FET



- In general, swing improves with thinner t_{Si}.
- Higher K → better swing.
- For ε=29, both types of swing can be less than 60 mV/dec MOSFET limit.

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Conclusion

- Subthreshold swing for silicon Tunnel FETs can go below 60mV/dec MOSFET limit.
- Optimization:
 - I_{on}/I_{off} ratio and S improved by high-K.
 - Optimum t_{Si} exists.
- 2D cross-sections show that gate controls whole body thickness.
- Tunnel FETs are promising for low standby power applications.