

Simulation of CMOS Nanotransistors

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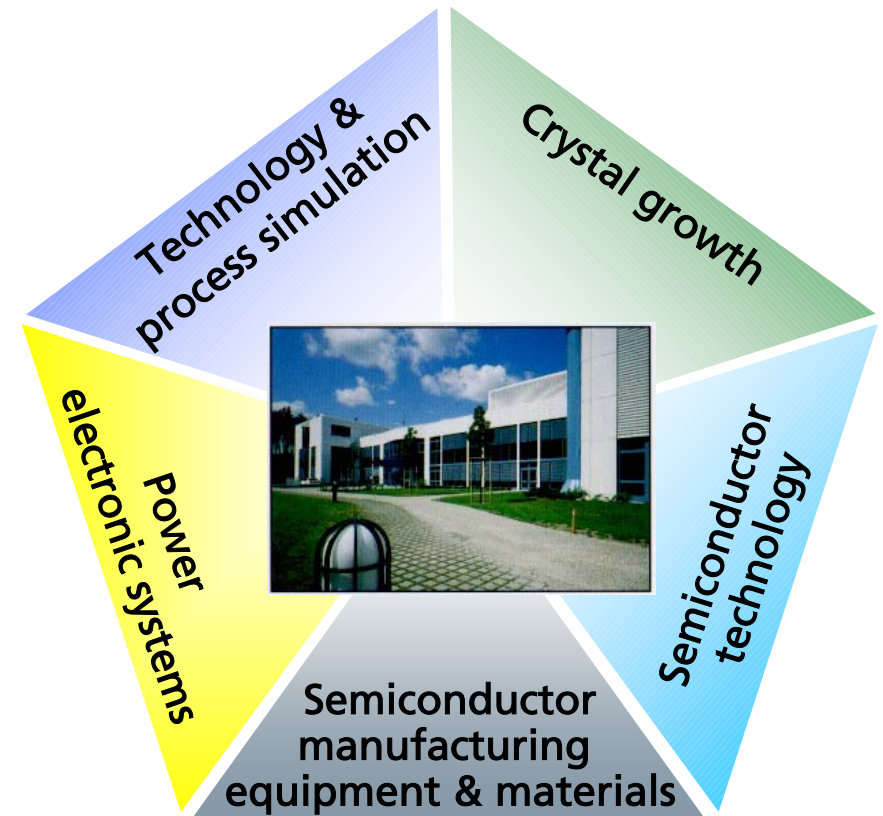
Introduction

Models and Software

Example: Device Scalability

Conclusions

Introduction: The Fraunhofer IISB in Erlangen



Introduction: Projects NanoCMOS and PullNano

NanoCMOS: CMOS backbone for 2010 e-Europe. From the 45 nm node down to the limits.

Project duration: March 2004 to May 2006

PullNano: Pulling the limits of NanoCMOS electronics

Project duration: June 2006 to June 2009

IISB Simulation

Process and device simulation, evaluation of novel device architectures, estimation of circuit-level performance of the project demonstrator



CMOS backbone for
2010 e-Europe
NANOCMOS

From the 45nm node down to the limits

Models and Software: New Effects – New Models

Standard device model

Drift-diffusion (DD) approximation, quasi-classical electron transport, electron properties as in bulk silicon

New effects

At small gate length new effects become important

- Velocity spectrum of electrons is far from that in thermal equilibrium
- Quantum mechanical effects
- Mechanical stress
- Parasitic resistances and capacitances

New models

Have to account for

- 1) velocity overshoot in short channel devices
- 2) quantum depletion in inversion layers
- 3) mechanical stress, parasitic effects

Models and Software: Model Choice

Electron transport

- Hydrodynamic (HD) approximation, electron and lattice temperatures
- Bude correction for the saturation velocity^{a)}

Quantum Effects

- Density Gradient (DG) approximation
- Modified local density approximation

Application area

Gate lengths: 50 to 10 nm; minimum silicon thickness: about 5 nm

Dimensionality

2D for wide channel bulk and double-gate transistors

3D for FinFETs and narrow channel MOSFETs

Software

Synopsys TCAD software suite

^{a)} J. D. Bude, SISPAD 2000, p23.

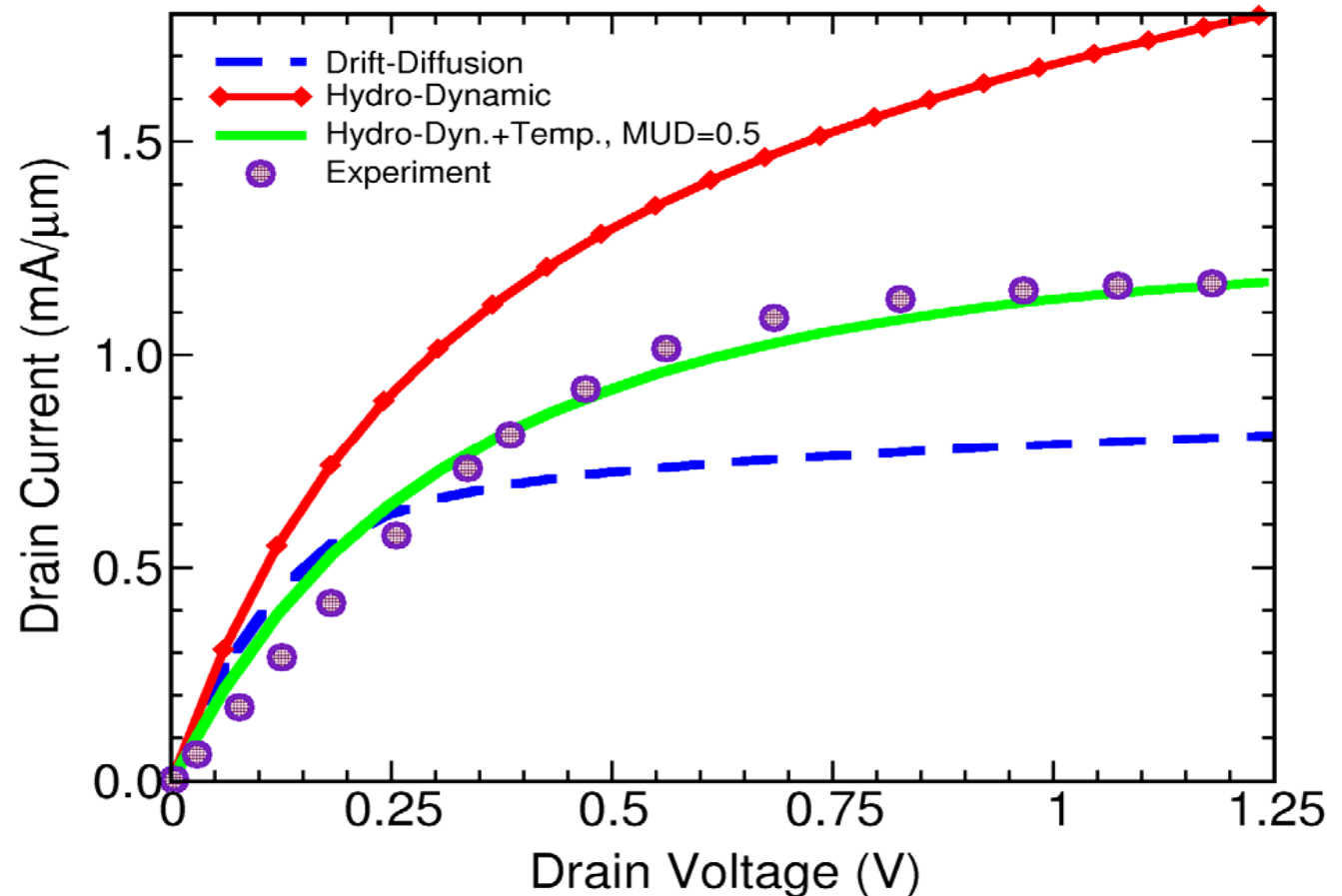
Verification of the Simulation Models (1)

Output characteristics of NMOS SOI transistors*) with a gate length of 40 nm

Experimental data are obtained for an undoped channel SOI, silicon thickness: 10 nm

Quantum effects: DG-model

Correction needed: surface roughness and phonon scattering related mobility reduced by a factor of 0.5



*) J. Kedzierski et al., IEDM 2003, p. 441

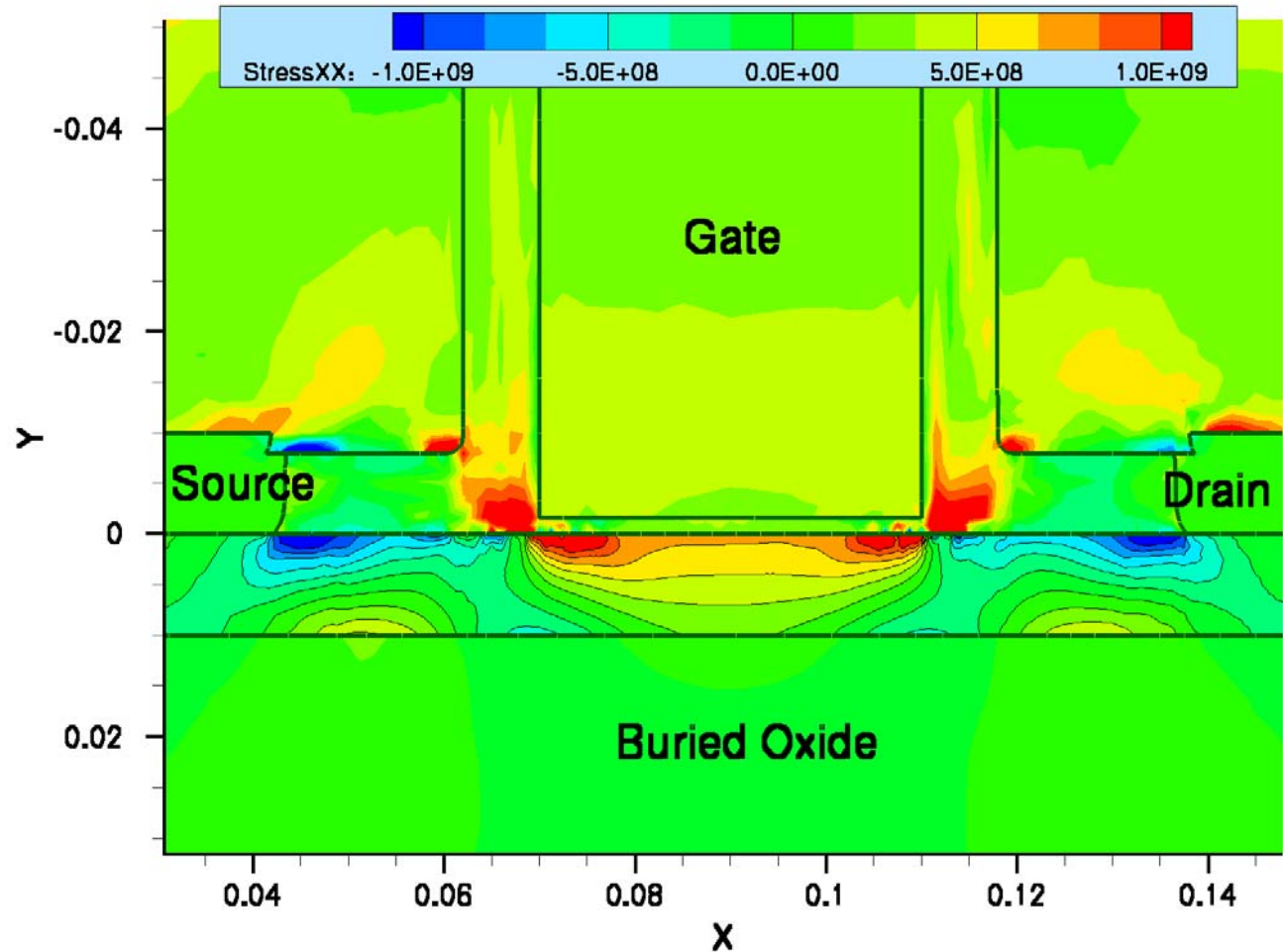
Verification of the Simulation Models (2)

Mechanical stress in an NMOS SOI transistor with a gate length of 40 nm

Stress component XX is due to forces in horizontal direction

Positive stress means dilatation, negative – compression

Positive XX-stress enhances electron mobility in silicon

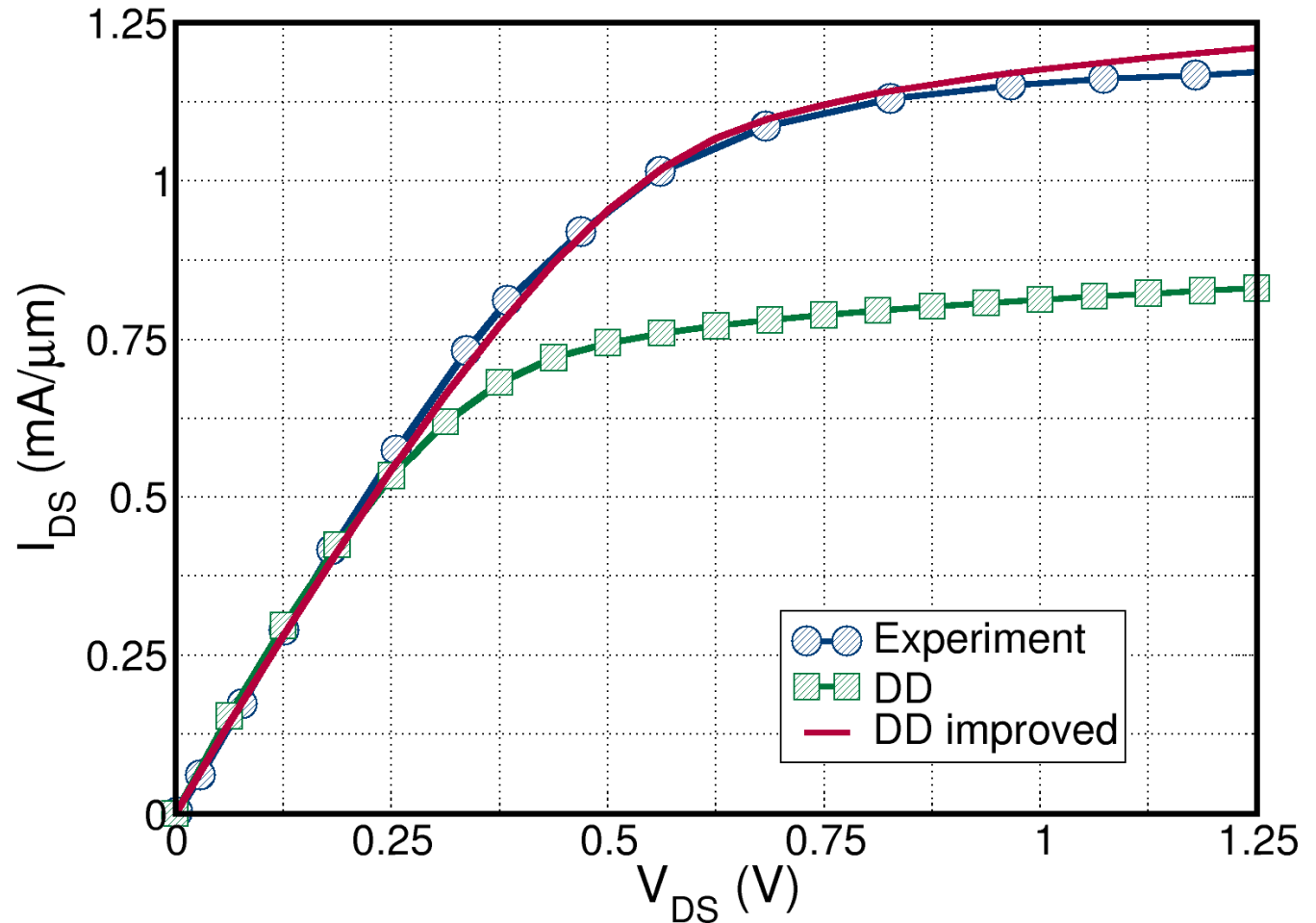


Verification of the Simulation Models (3)

Transfer characteristics of a CMOS SOI transistor with a gate length of 40 nm

Experimental data are obtained for an undoped channel SOI, silicon thickness: 10 nm

Good reproduction of measured data, if contact resistances and mechanical stress are taken into account in the simulations



Experiment: J. Kedzierski et al.,
IEDM 2003, p. 441

Example: Scalability of Different MOS Transistors

Devices

Conventional bulk NMOSFET

Double-gate SOI NMOSFET

Triple-gate N-channel FinFET

Scaling

From gate length of 25 nm down to gate lengths of 12 nm

Constraint

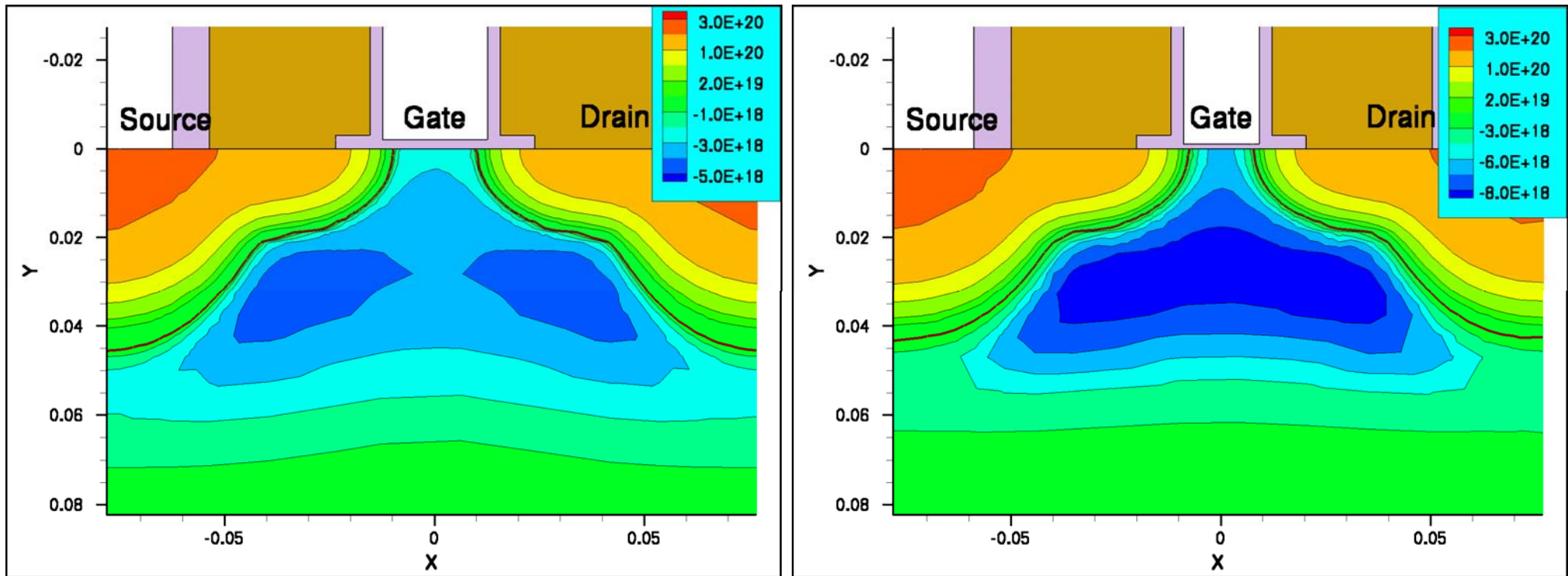
Gate oxide thickness not thinner than 1 nm

Supply Voltage

The same supply voltage of 1 V applied to all devices for an easy comparison

Conventional bulk MOS Transistors

Doping distribution in NMOS bulk transistors with a gate length of 25 nm (left) and 18 nm (right)



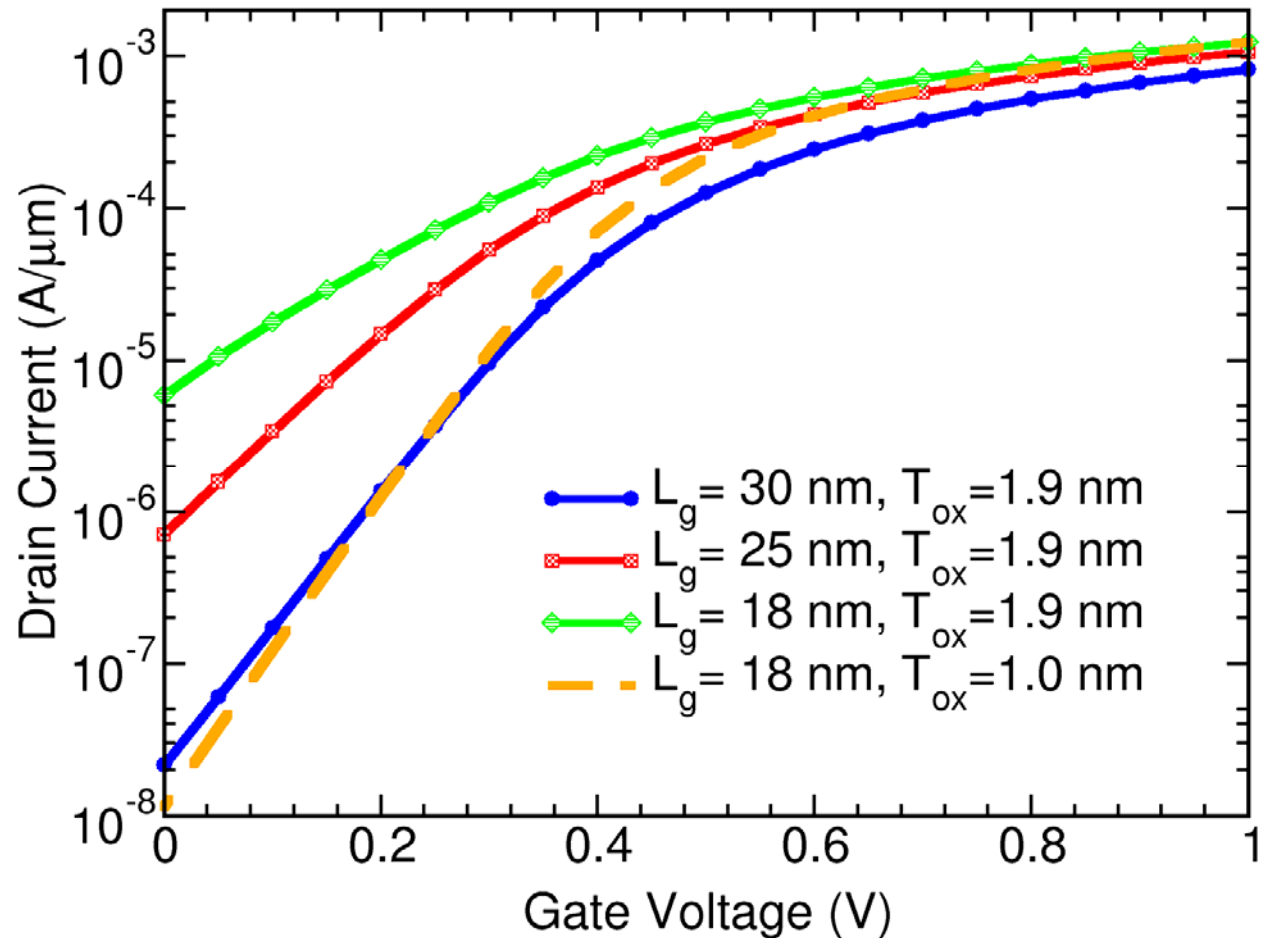
Conventional bulk MOS Transistors

Transfer characteristics of bulk NMOS transistors when scaling from a gate length of 25 nm to 18 nm

$L_g=30 \rightarrow 25$ nm: no other change

$L_g=25 \rightarrow 18$ nm: higher channel doping level

$L_g=18$ nm: thinner gate oxide improves performance



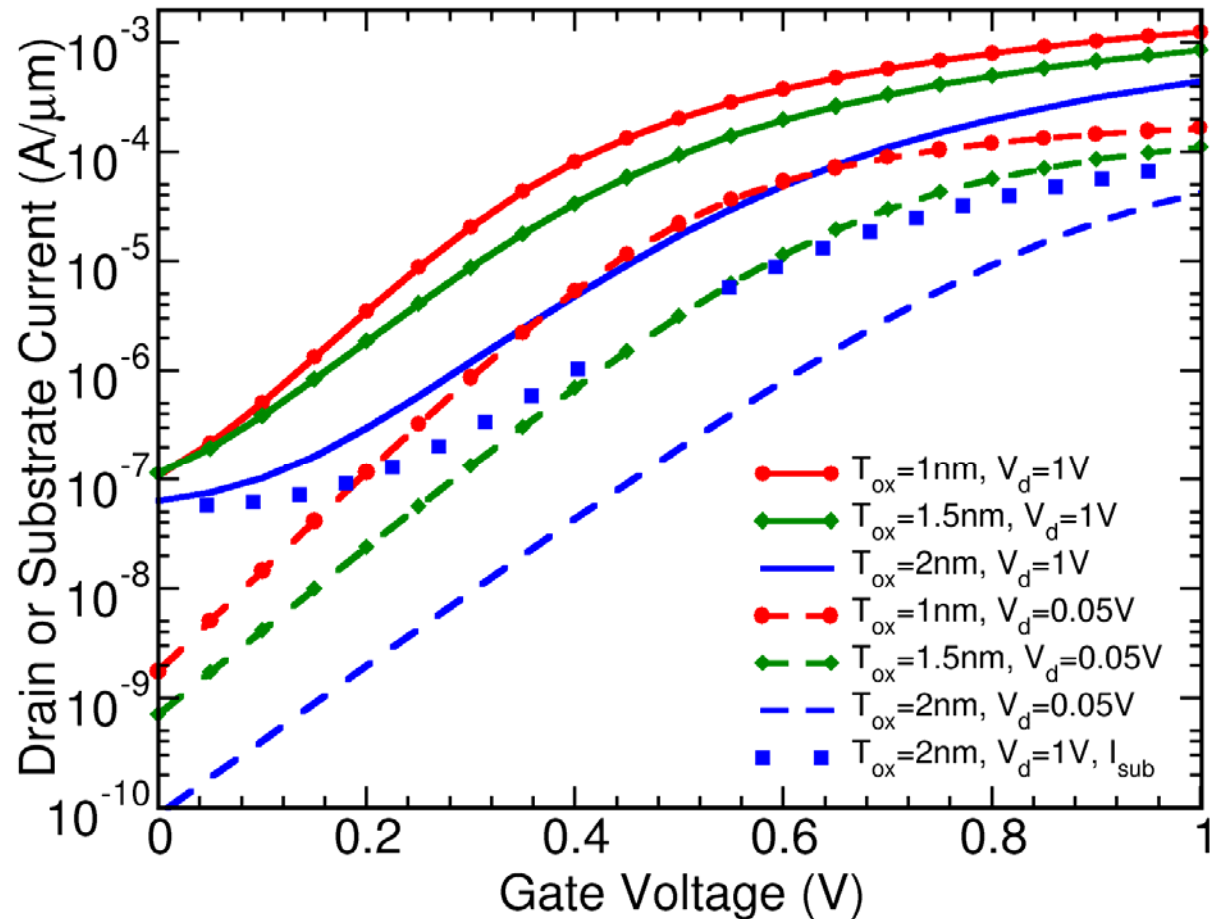
Conventional bulk MOS Transistors

Transfer characteristics of bulk NMOS transistors for a gate length of 12 nm

$L_g=12$ nm: thinner gate oxide only slightly improves performance

High leakage current remains even at gate oxide thickness of 1 nm

Large DIBL effect of about 200 mV/V



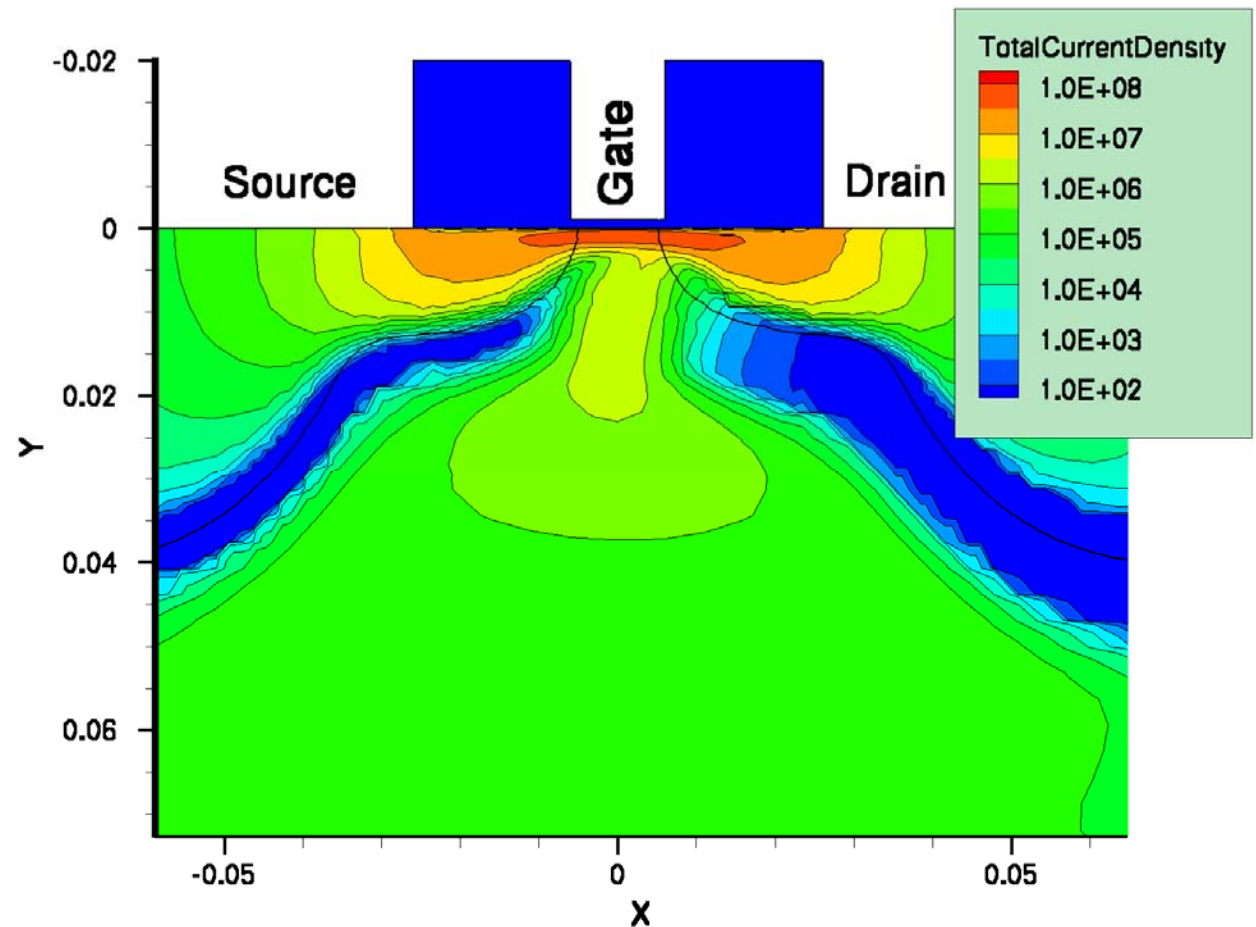
Conventional bulk MOS Transistors

Current density in a bulk NMOS transistor with a gate length of 12 nm

Electrically open transistor
Gate and drain voltage: 1 V

A strong path of parasitic current from channel to the substrate is seen

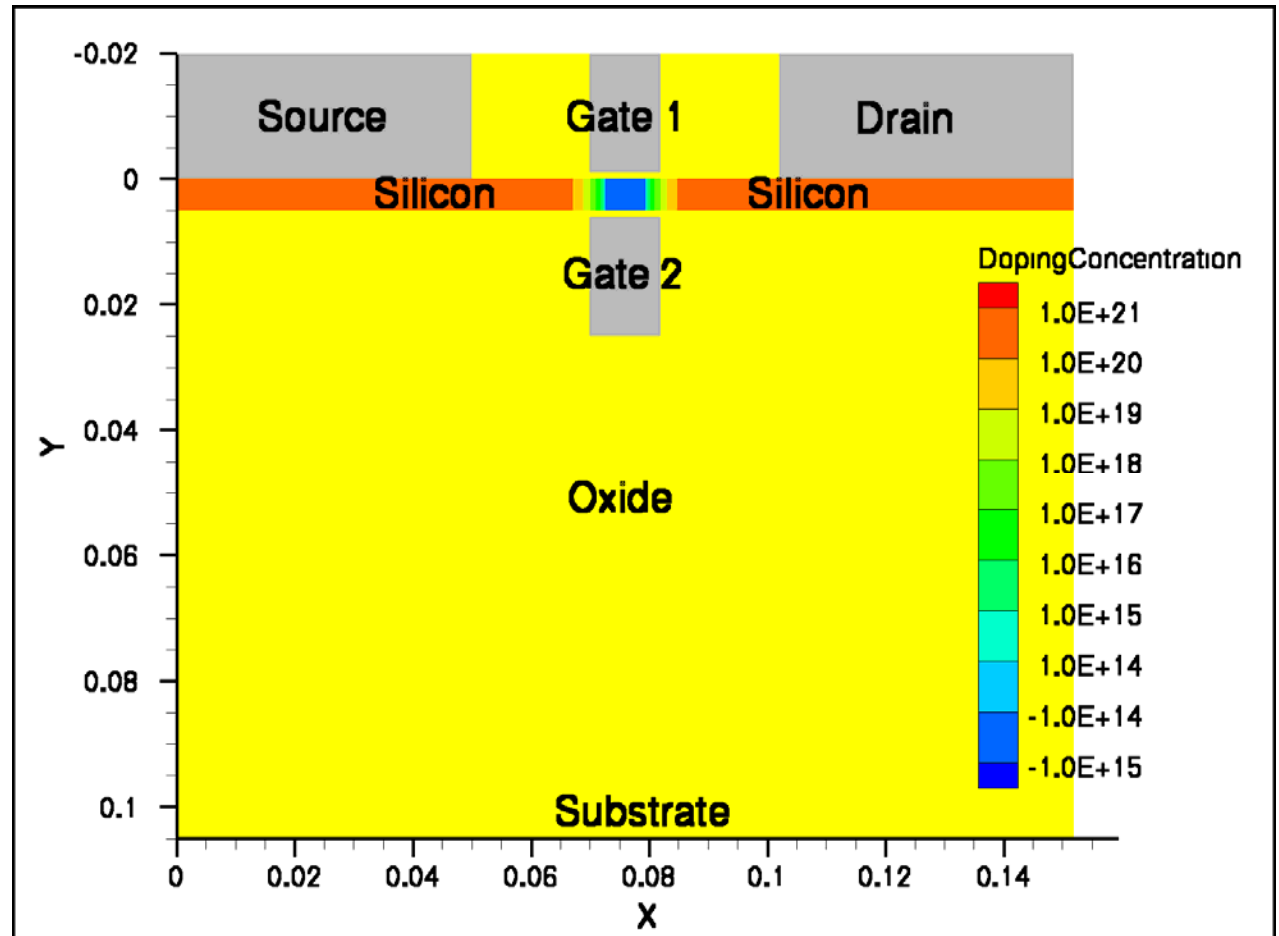
This parasitic leakage current is due to impact ionization



Double-Gate SOI MOS Transistors

Geometrical shape and doping distribution in a double-gate NMOS transistor with a gate length of 12 nm

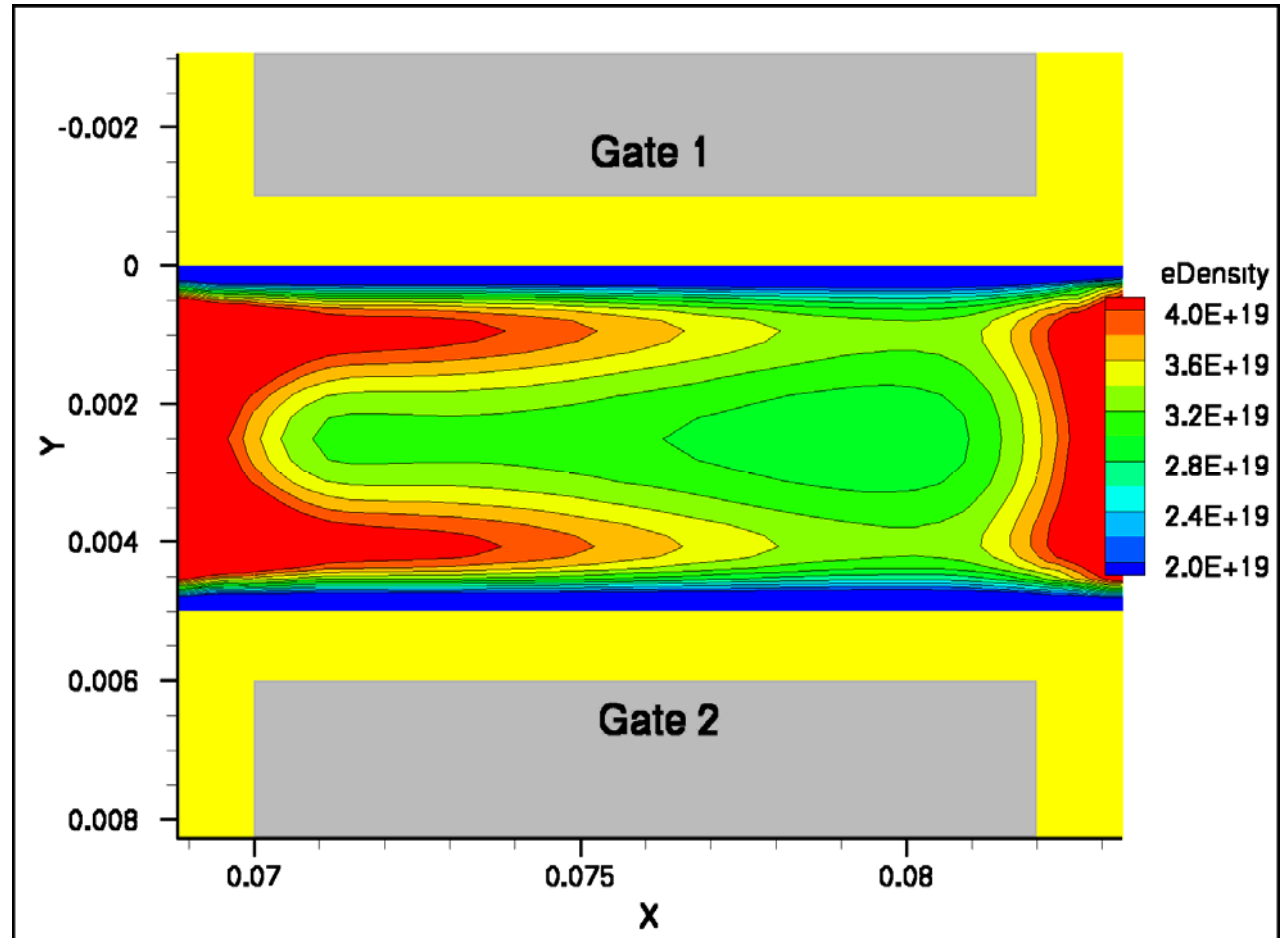
- Undoped channel
- Silicon thickness: 5 nm
- Buried oxide: 100 nm
- Ideally aligned double gate



Double-Gate SOI MOS Transistors

Distribution of electron density in a double-gate NMOS transistor with a gate length of 12 nm

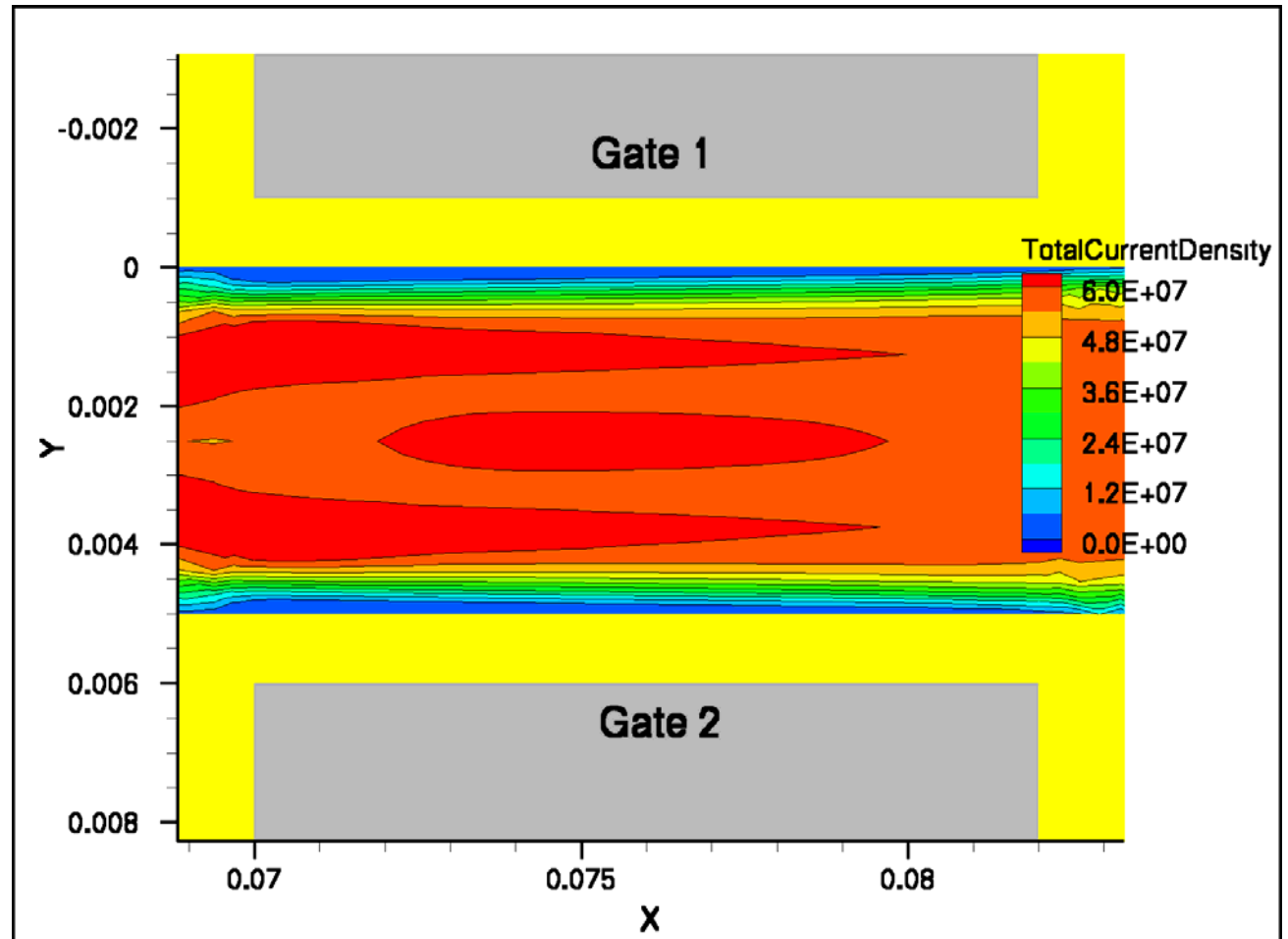
- Gate and drain voltage: 1 V
- Double peak distribution
- Significant overlap of the inversion layers from both gates
- Strong quantum depletion near the gates



Double-Gate SOI MOS Transistors

Distribution of current density in a double-gate NMOS transistor with a gate length of 12 nm

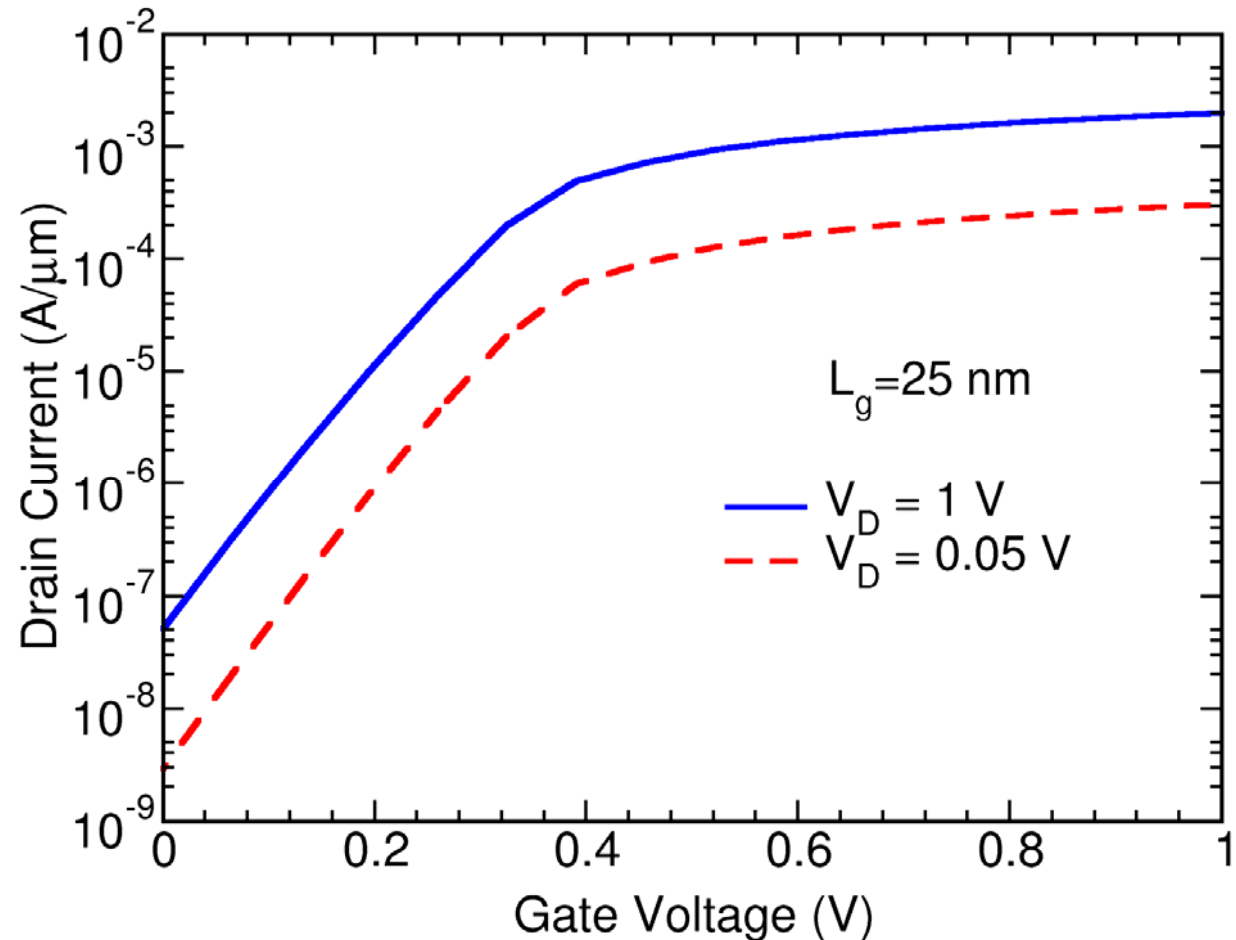
- Gate and drain voltage: 1 V
- Almost uniform distribution of current: Volume inversion
- Strong quantum depletion near the gates



Double-Gate SOI MOS Transistors

Transfer characteristics of double-gate NMOS transistor with a gate length of 25 nm

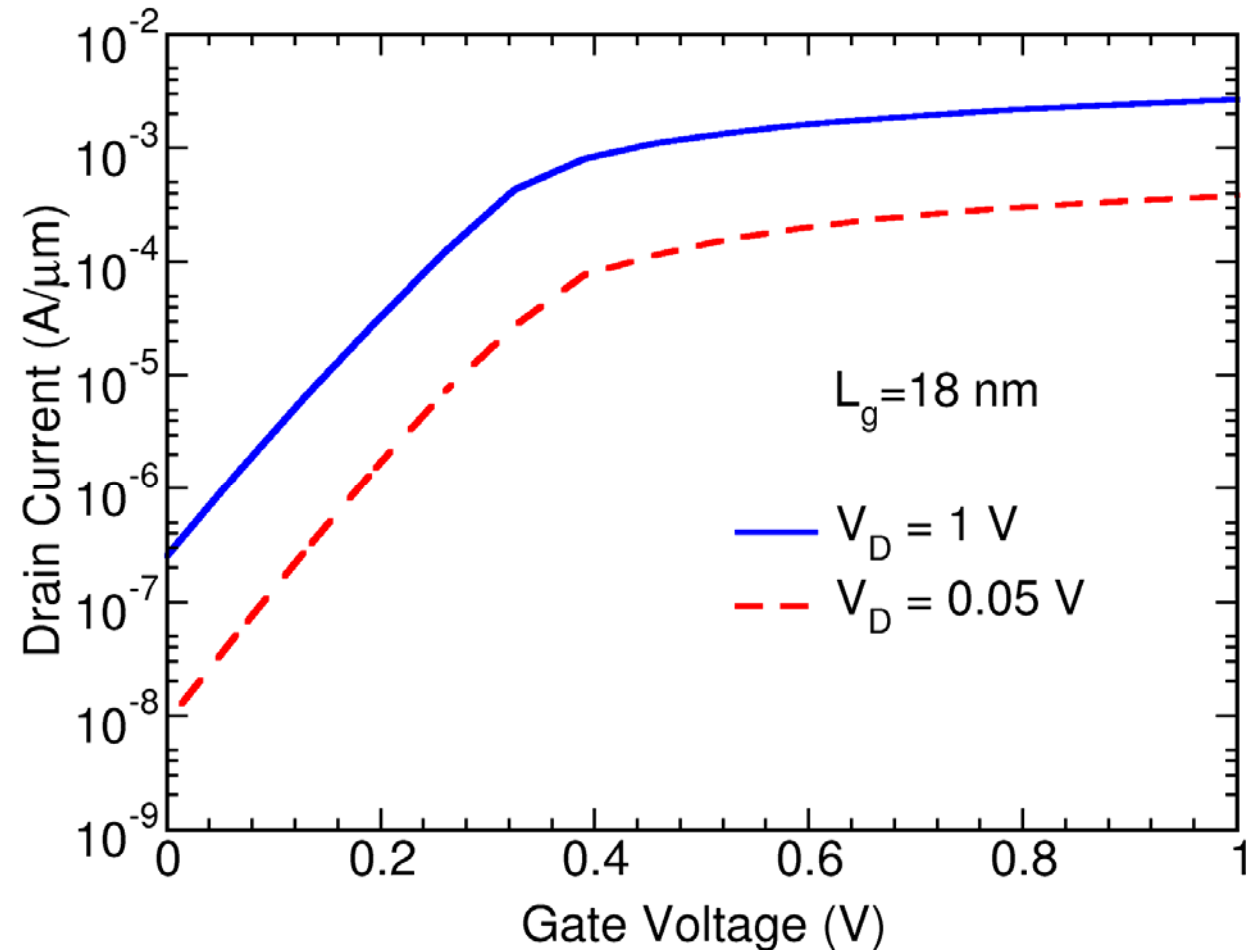
- Undoped channel
- Silicon thickness: 10 nm
- Gate oxide: 1.5 nm
- Subthreshold slope: 82 mV/dec
- DIBL: 103 mV/V



Double-Gate SOI MOS Transistors

Transfer characteristics of double-gate NMOS transistor with a gate length of 18 nm

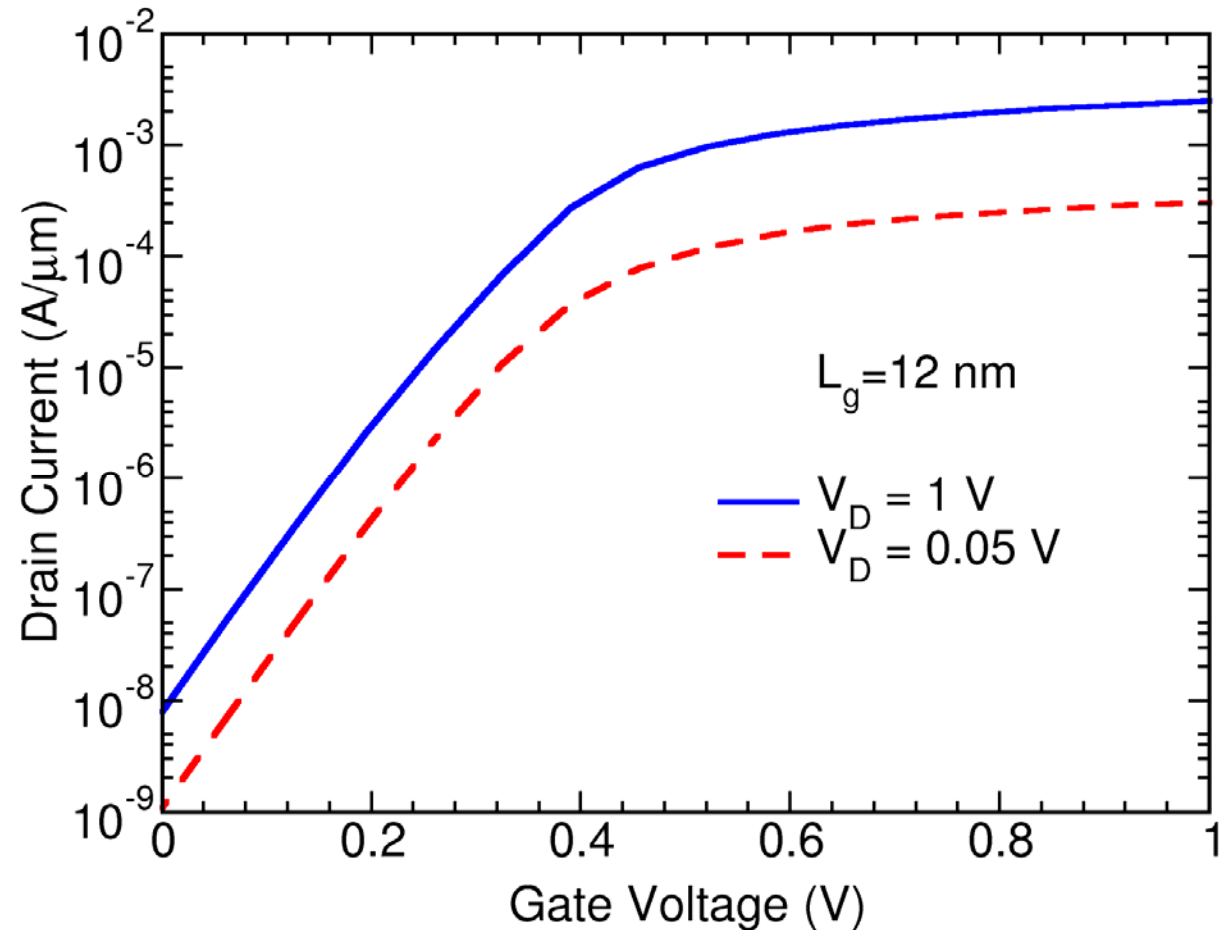
- Undoped channel
- Silicon thickness: 10 nm
- Gate oxide: 1.0 nm
- Subthreshold slope: 90 mV/dec
- DIBL: 133 mV/V



Double-Gate SOI MOS Transistors

Transfer characteristics of double-gate NMOS transistor with a gate length of 12 nm

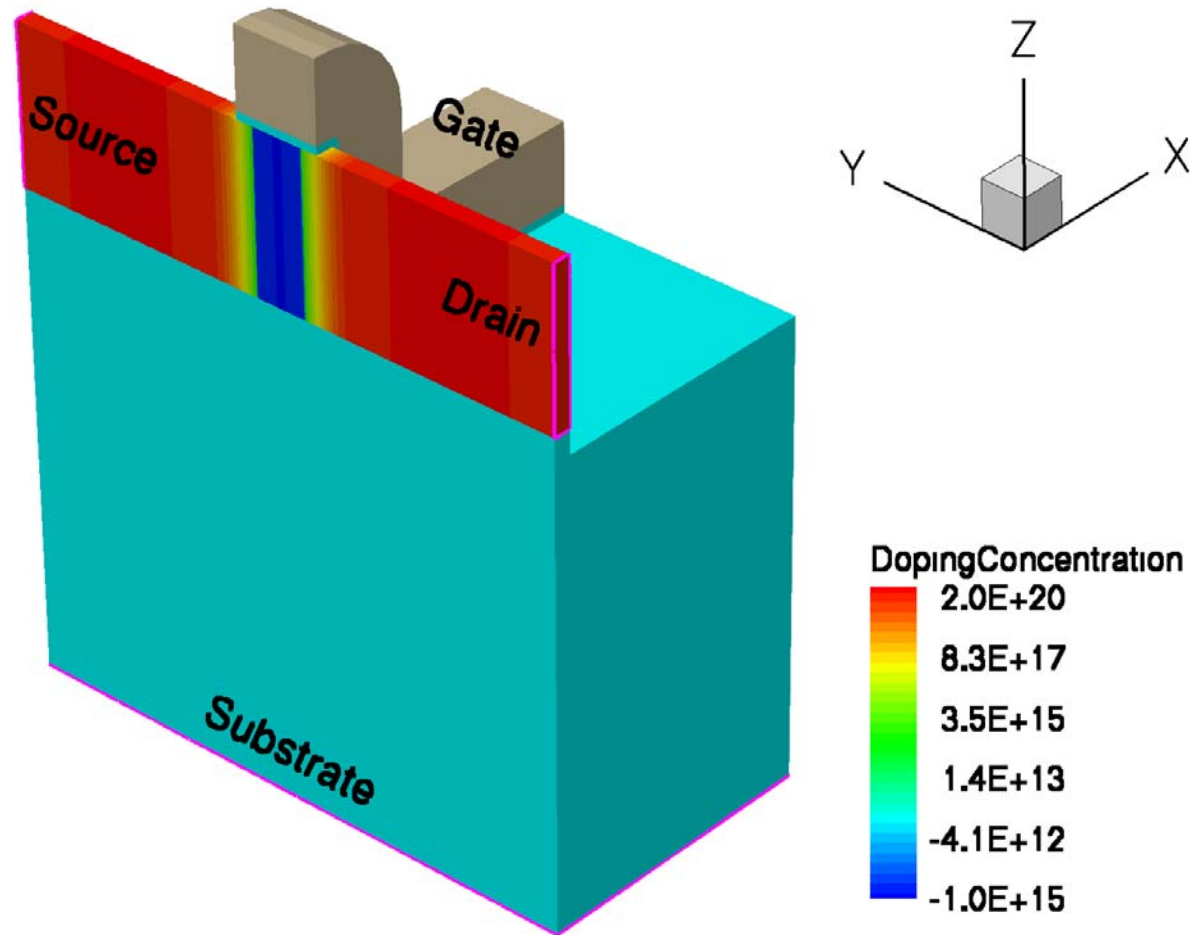
- Undoped channel
- Silicon thickness: 5 nm
- Gate oxide: 1.0 nm
- Subthreshold slope: 76 mV/dec (thinner oxide)
- DIBL: 71 mV/V



Triple-Gate FinFETs

Geometrical shape and doping distribution in a FinFET with a gate length of 12 nm

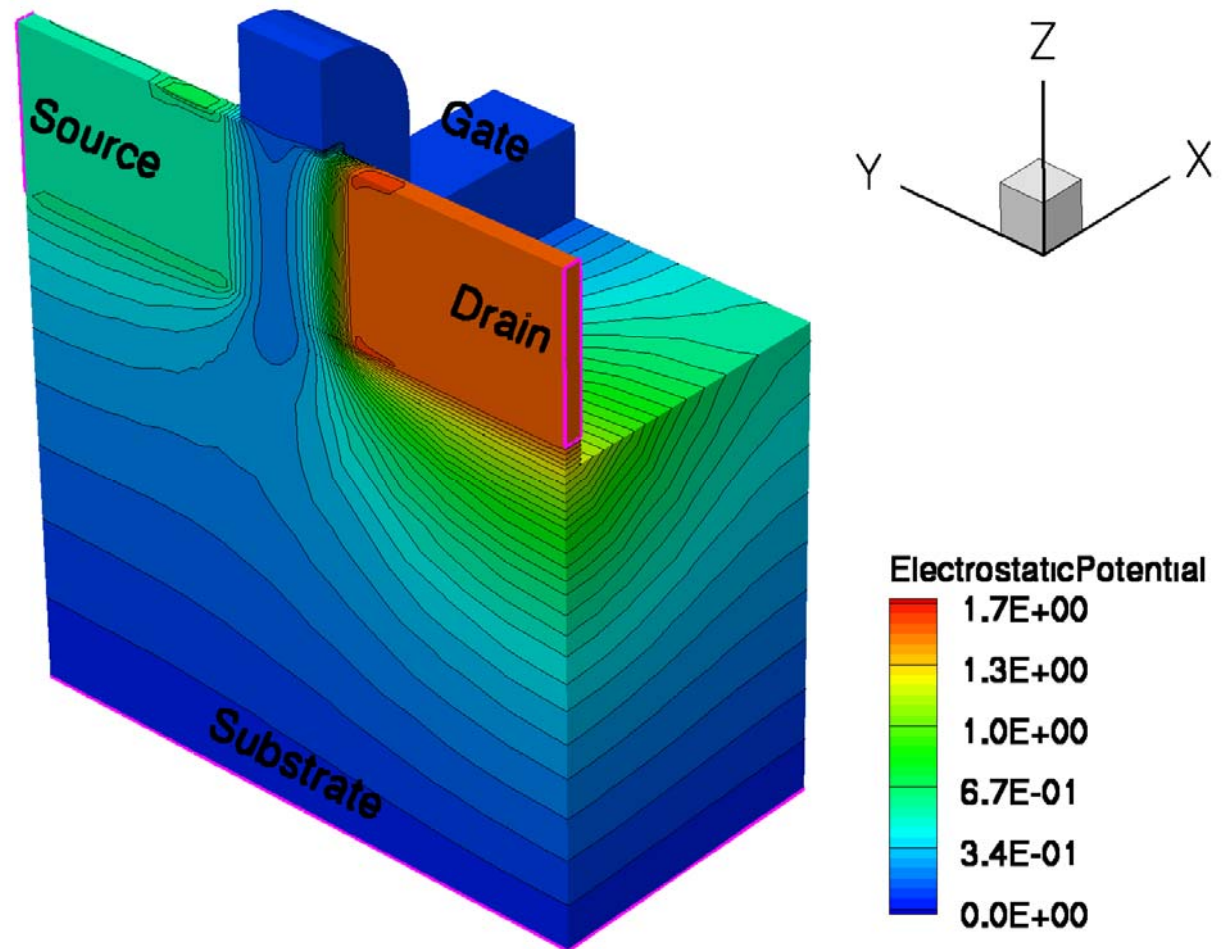
- Undoped channel
- Silicon thickness: 5 nm
- Gate oxide: 1.0 nm
- 3D simulation is needed because of the geometrical shape



Triple-Gate FinFETs

Potential distribution in an electrically closed FinFET with a gate length of 12 nm

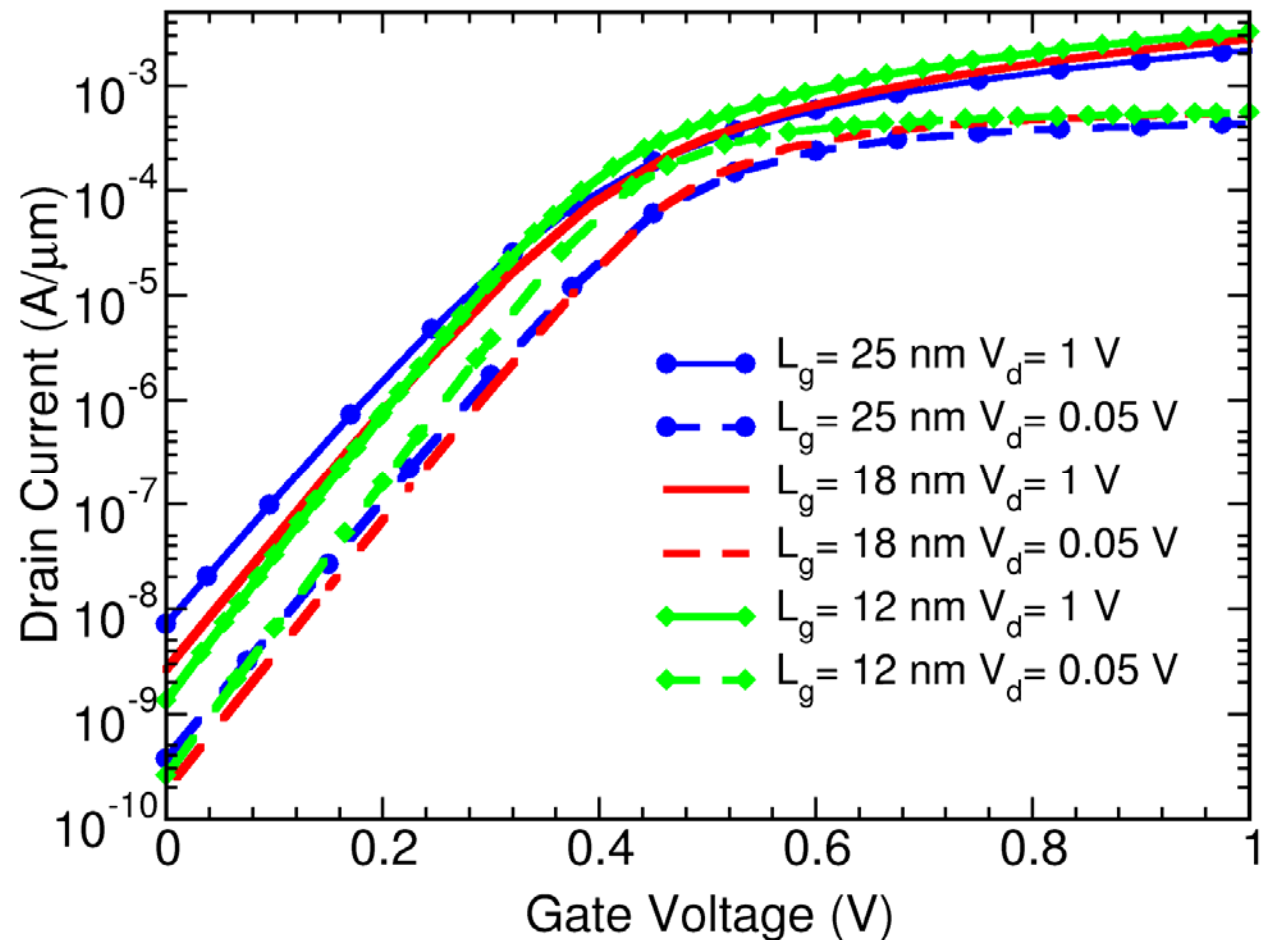
- Undoped channel
- Silicon thickness: 5 nm
- Gate oxide: 1.0 nm
- Gate voltage: 0 V
- Drain voltage: 1 V



Triple-Gate FinFETs

Transfer characteristics of N-channel FinFETs with a gate lengths of 25, 18, and 12 nm

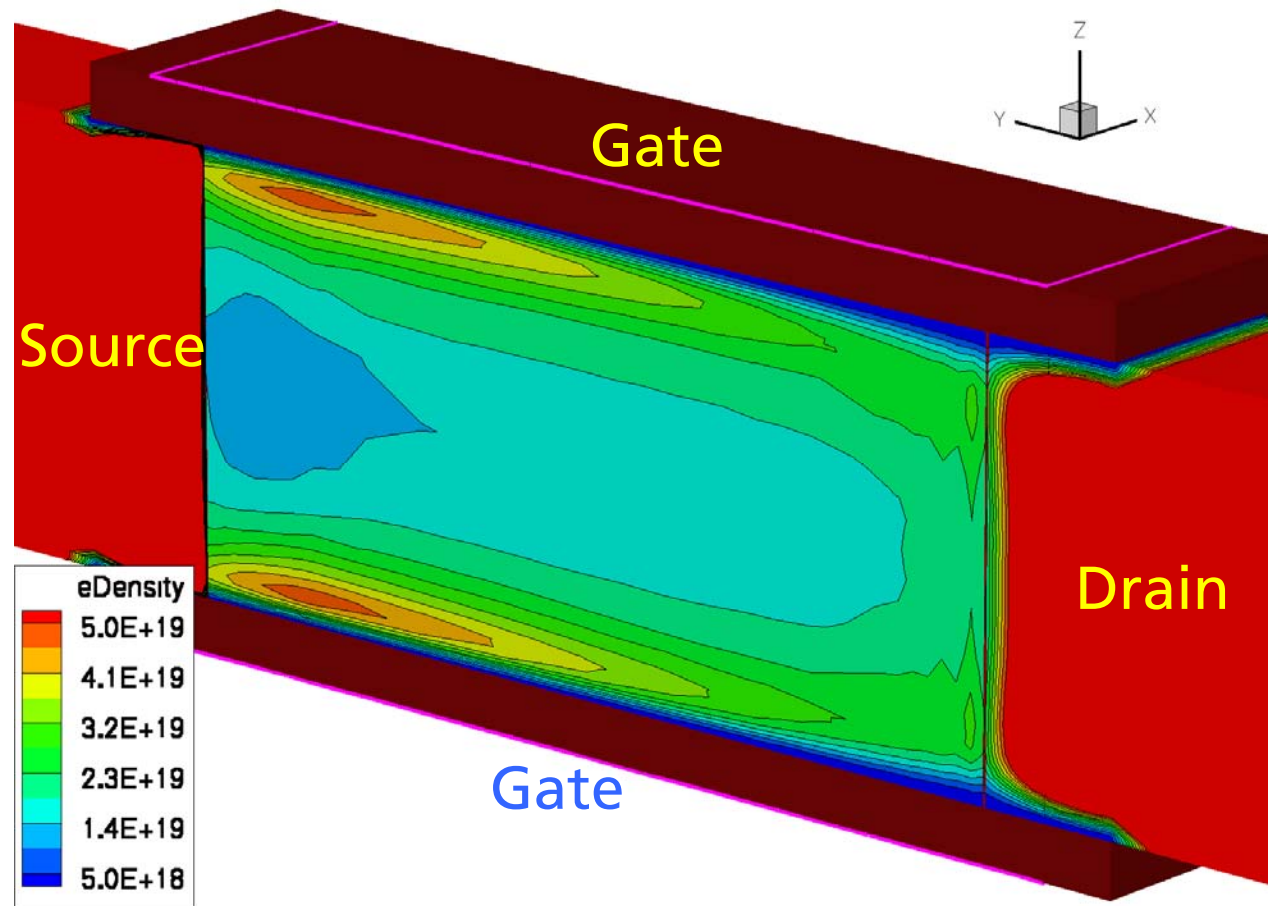
- Best performance at gate length of 12 nm
- Subthreshold slope: 72 mV/dec
- DIBL: 52 mV/V
- $I_{on}/I_{off}=2.34 \cdot 10^6$ @ 1V supply voltage



Gate-All-Around FinFETs (Nanowires)

Electron density in an GAA FinFET with a gate length of 21 nm

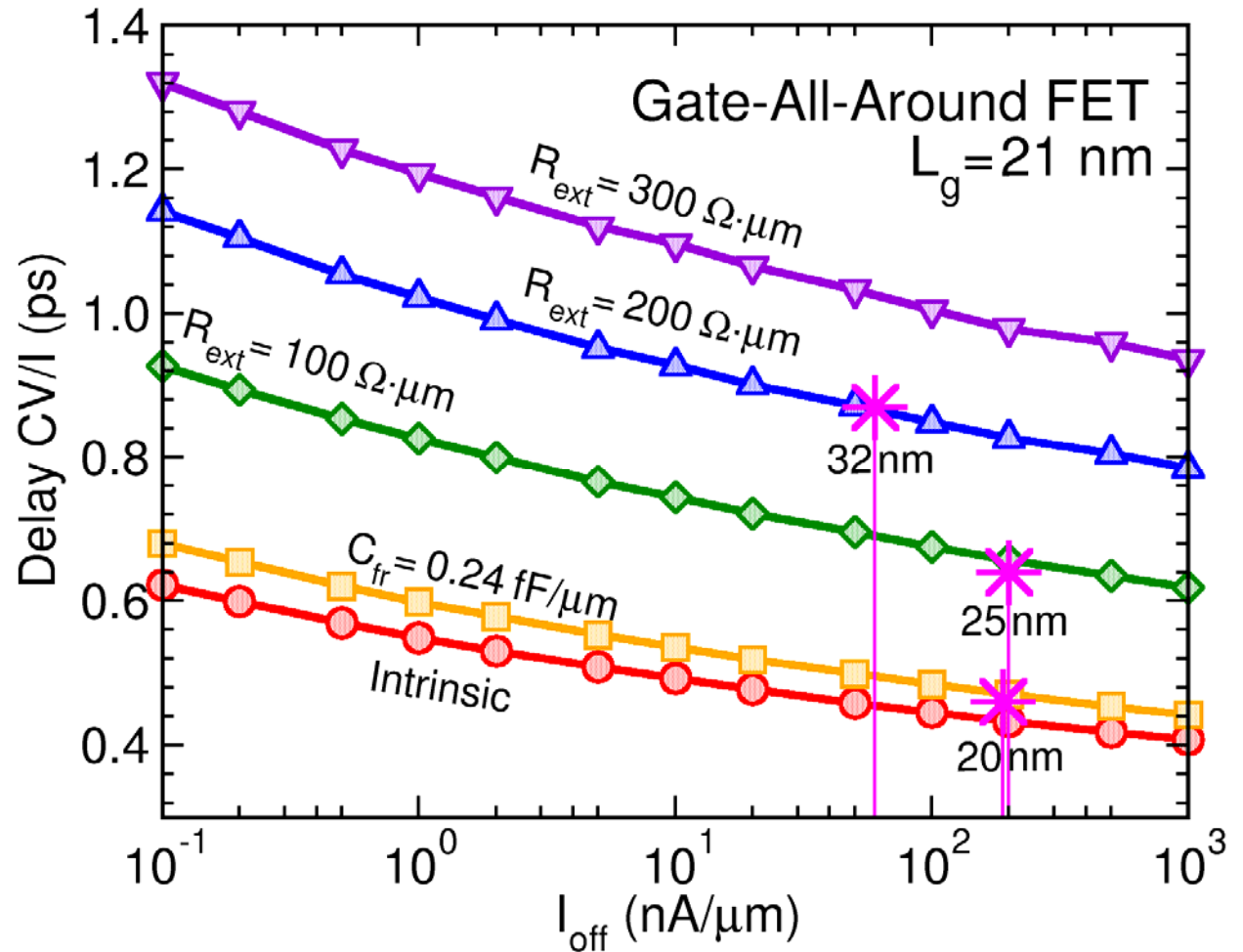
- Gate and drain contacts are at supply voltage
- One half of transistor shown
- Two inversion layers are seen in the cut plane
- Quantum mechanical depletion near the gate oxide is observed



Gate-All-Around FinFETs

Gate Delay of GAA FinFETs

- Stars: ITRS specifications for intrinsic gate delay for gate lengths indicated by numbers
- Intrinsic gate delay satisfy the ITRS specifications
- Contact resistance R_{ext} has a large impact on the gate delay
- Effect of parasitic fringing capacitance C_{fr} is seen



Conclusions

- The necessity to apply complex device simulation models which include several new physical effects in nanometer scaled CMOS devices was shown
- The improved simulation models have been verified against experimental measurements on bulk CMOS and on thin SOI CMOS transistors
- Mechanical stress has to be included into the simulation of nano-scaled MOS transistors to reproduce the measured transistor performance
- Scalability of three CMOS device architectures: bulk MOS, double-gate SOI MOSFET, and FinFET for gate lengths from 25 to 12 nm were investigated using numerical simulation
- Parasitic resistances associated with contacts seriously limit the dynamic performance of nanotransistors. Especially large is the effect of parasitic resistances in thin silicon nano-wire transistors